

ESDA/JEDEC JTR002-01-25

ESDA/JEDEC Joint Technical Report

ESDA/JEDEC JTR002-01-25
A revision of ESDA/JEDEC JTR002-01-22



*For the User Guide of
ANSI/ESDA/JEDEC JS-002*

*Charged Device Model Testing of
Integrated Circuits*

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FOREWORD

This technical report¹ is intended to be a complimentary document to ANSI/ESDA/JEDEC JS-002. The intention of this document is to act as a user guide for JS-002 and give the user a wealth of additional information to help them execute CDM testing within their company. This document covers some basic practical considerations such as cleaning and cable replacement and digs into more detailed discussions regarding the oscilloscope and handling charging delays. It also gives a detailed discussion on waveform verification that gives the user a clear/concise approach to completing waveform verification with waveform examples included. This is followed by guidance on the impacts of package size on the peak current, the ability to calculate the charge associated with a waveform discharge, and some practical guidance and ways to handle difficult-to-test packaging that should prove to be very helpful to the user. The final sections address some of the challenges with no-connects, the first pin tested risks, and wraps up with a discussion on reporting CDM data to the customer. The intent is to update this technical report in the future as the joint CDM WG finds new learnings, and each time ANSI/ESDA/JEDEC JS-002 is updated.

Additionally, the option of using a 1-GHz oscilloscope has been removed from the JTR002 document in the JTR002-01-23 revision, including any references to the 1-GHz verification method. The option to use the 1-GHz oscilloscope, which was initially left in the ANSI/ESDA/JEDEC JS-002 joint standard in previous versions of ANSI/ESDA/JEDEC JS-002 as it was in the JESD22-C101 standard, has been removed in ANSI/ESDA JEDEC JS-002-2024. The higher bandwidth oscilloscope (6-GHz bandwidth or greater) provides a more realistic representation of the CDM discharge waveform.

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¹ **Technical Report (TR):** A collection of technical data or test results published as an informational reference on a specific material, product, system or process.

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**ESDA/JEDEC Joint Technical Report for the User Guide of ANSI/ESDA/JEDEC JS-002
Charged Device Model Testing of Integrated Circuits**

1.0 PURPOSE AND SCOPE

1.1 Purpose

The information and procedures defined in this technical report are intended to help users better understand the procedures and requirements specified in ANSI/ESDA/JEDEC JS-002.

1.2 Scope

This report only covers the procedures and requirements specified in ANSI/ESDA/JEDEC JS-002.

2.0 REFERENCED PUBLICATIONS

Unless otherwise specified, the following documents of the latest issue, revision, or amendment form a part of this standard to the extent specified herein:

ESD ADV1.0. ESD Association Glossary of Terms²

ANSI/ESDA/JEDEC JS-002, For Electrostatic Discharge Sensitivity Testing Charged Device Model (CDM) Device Level^{2,3}

3.0 PERSONNEL SAFETY

THE EQUIPMENT SHALL NOT BE INSTALLED OR OPERATED IN A COMBUSTIBLE (HAZARDOUS) ENVIRONMENT.

3.1 Training

ALL PERSONNEL SHOULD RECEIVE SYSTEM OPERATIONAL TRAINING AND ELECTRICAL SAFETY TRAINING BEFORE USING THE EQUIPMENT.

3.2 Personnel Safety

THE PROCEDURES AND EQUIPMENT DESCRIBED IN THIS DOCUMENT MAY EXPOSE PERSONNEL TO HAZARDOUS ELECTRICAL CONDITIONS. USERS OF THIS DOCUMENT ARE RESPONSIBLE FOR SELECTING EQUIPMENT THAT COMPLIES WITH APPLICABLE LAWS, REGULATORY CODES, AND BOTH EXTERNAL AND INTERNAL POLICY. USERS ARE CAUTIONED THAT THIS DOCUMENT CANNOT REPLACE OR SUPERSEDE ANY REQUIREMENTS FOR PERSONNEL SAFETY.

GROUND FAULT CIRCUIT INTERRUPTERS (GFCI) AND OTHER SAFETY PROTECTION SHOULD BE CONSIDERED WHEREVER PERSONNEL MIGHT COME INTO CONTACT WITH ELECTRICAL SOURCES.

ELECTRICAL HAZARD REDUCTION PRACTICES SHOULD BE EXERCISED, AND PROPER GROUNDING INSTRUCTIONS FOR EQUIPMENT SHALL BE FOLLOWED.

NOTE: CDM TESTERS HAVE MOVING PARTS WHEN IN OPERATION AND CARE SHOULD BE TAKEN TO AVOID PERSONNEL CONTACT WITH MOVING PARTS WHEN IN OPERATION.

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4.0 CDM TESTER OPERATIONAL CONSIDERATIONS

4.1 Cleaning

4.1.1 Tester Cleaning

Waveform performance can be affected by contamination on any part of the test system, including the field plate dielectric, calibration targets, ground plane pogo pin, and the device under test.

Use isopropanol (isopropyl alcohol, IPA) to clean each item listed below using a procedure approved by the local safety organization and avoiding leaving any residue:

- The calibration targets should be properly stored when not in use. These should be cleaned before being used for waveform verification, using either a lint-free cloth or swab.
- The field plate dielectric should be cleaned using a lint-free cloth to ensure no fibers are left on the plate. Care should be taken when cleaning around the vacuum holes. It is best to clean this area with a swab.
- The ground plane pogo pin should be cleaned using a swab, and care should be taken to avoid damaging the pogo pin with excessive force or using too much alcohol as this may remove the lubricant within the pogo pin body.

4.1.2 Device Cleaning

Care should be taken when handling all components of the system and devices to be tested. To avoid depositing oils from your fingers on the package pins, use ESD handling practices consistent with the company's ESD handling procedures such as dissipative tweezers or vacuum wands. Direct contact between the package pins and skin should be avoided, if possible, to minimize contamination.

Devices should be cleaned with IPA and allowed to dry prior to being placed in the tester. Cleaning of the device improves waveform repeatability during CDM testing by minimizing contaminants. Use a procedure approved by the local safety organization and following internal ESD procedures. A soft brush can be used to gently clean the device terminals paying attention to avoid bending pins or removing balls. Devices should then be handled in a way that maintains cleanliness (vacuum tweezers, personnel wearing finger cots or equivalent, or plastic tweezers, which have been neutralized by holding in an ionized air stream). Cleaning with isopropyl alcohol may leave the surface moist for some time after the cleaning. The moisture may provide an unintended leakage path if present during the stress. It is important to dry all surfaces after cleaning, either by allowing the surfaces to dry naturally or using forced air to evaporate the moisture.

Packages with an open cavity (for example, microphones) should be cleaned with particular attention to avoid IPA leaking into the package cavity. If this cannot be done, let the package dry longer after cleaning.

NOTE: The cleaning process may be verified by stressing and measuring the peak current on several cleaned parts, comparing the same pins for peak current consistency.

4.2 Routine Versus Quarterly Checks

ANSI/ESDA/JEDEC JS-002 specifies that waveforms should be verified at least once per shift when CDM testing is performed. This does not require a full waveform verification but typically uses one verification module at the most common Test Condition planned. The verification module which most closely matches the packaged device's capacitance to the field plate should be used. However, determining the package capacitance can be time-consuming. For routine waveform verification of one Test Condition, choosing the verification module most closely aligned to the package size is reasonable. As shown in Section 7.0, if one verification module is aligned to the center of the I_{peak} range, likely, the other verification module is aligned. If there is any doubt, complete the routine verification using both verification modules. This ensures the tester and waveforms meet the required specifications, and the tester is operating within tolerances between full waveform verifications. Longer periods between routine waveform verifications are allowed. It is important to note that the longer the time between waveform verifications, the more CDM results to be in question should an issue be found during routine waveform verification.

In addition to the daily routine checks, waveform verifications should be performed quarterly or when changes are made to the system hardware or portions of the measurement chain (for example, replacing the pogo pin).

Quarterly waveform verifications are similar to routine verifications but include all Test Conditions, both polarities, and both verification modules as a requirement. It is important to record the data when performing these measurements to prove the system is within specifications.

4.2.1 Tracking Factor/Offset Settings

As current waveform amplitudes are based on the voltage factor and offset settings, it is recommended that these values be captured when performing the routine or quarterly verifications. These factor/offset settings should be reviewed. If these settings are increasing or decreasing over time, it may indicate an issue with the system.

4.2.2 Hardware Changes Requiring Waveform Verification

Many CDM test systems offer configurations to meet multiple CDM test standards. Waveforms must be verified when switching between these configurations, ensuring the tester hardware meets the given standard requirements. For example, the legacy ESDA and AEC standards used a thin insulator between the field plate and the device under test (DUT). In contrast, ANSI/ESDA/JEDEC JS-002 uses a 0.381 mm \pm 0.025 mm (15 mil) thick FR4 field plate dielectric between the field plate and the DUT.

Other hardware changes, such as replacing the discharge pogo pin, require that a complete verification be performed. Pogo pins have a limited life, which may be as little as six months, depending on usage. Routine daily waveform verification may show changes in the waveforms as the pogo pin deteriorates. Changes in the shape of the waveform can be a good indication that the pogo pin needs to be replaced.

NOTE: Manufacturers' recommendations should be followed when removing and replacing a pogo pin. It is important to measure the length of the exposed portion of the pogo pin before removing it from the socket to ensure the same length can be set when installing the new pogo pin.

4.3 Holding a Package in Place, Z Height Caution

Field induced CDM testing requires the device to be in a dead bug position (upside down) on the field plate dielectric. Vacuum holes in the field plate/dielectric are used to hold the device in place during testing. However, in some cases, the device may have to be held in place or supported by a fixturing material similar to the FR4 epoxy board used for the field plate dielectric. Section 14.0, Small Package Parts and CDM, discusses the use of FR4 to hold very small devices in place during testing.

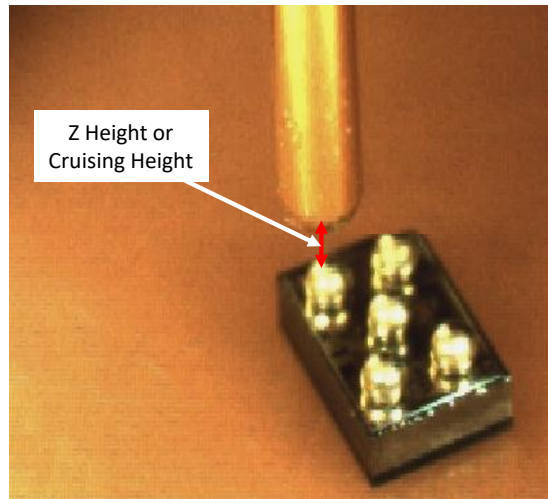


Figure 1: Relative Position (Z Height or “Cruising Height”) of the Pogo Pin to the DUT During the Movement from Pin to Pin During Testing

CDM test systems use X and Y mechanisms to position the ground (discharge) pogo pin over the pin to be tested and a Z mechanism to contact the pogo pin and the pin under test. When moving from pin to pin on the device, the pogo pin is moved away from the device, and the X and Y mechanisms position the pogo pin over the next pin to be tested. Enough space must be left between the device pins and the ground pogo pin when the X and Y mechanisms are moving to avoid hitting a pin on the device and possibly damaging the device or simply moving the device, which would require repositioning the device to continue testing.

The picture above in Figure 1 shows an example of the Z height clearance between the pogo pin and a device under test. As the BGA device has only one ball height, it is easy to set an appropriate repositioning Z height, or as it is referred to in some test systems as “cruising height”. When a device has different height pins, it is important to set this “cruising height” high enough that the pogo does not hit any pins or even the device body during the X and Y movements. The photo below in Figure 2 shows an example of a device where it would be important to set the “cruising height” properly to avoid hitting the components in the center of the grid during the X and Y movement from pin to pin.

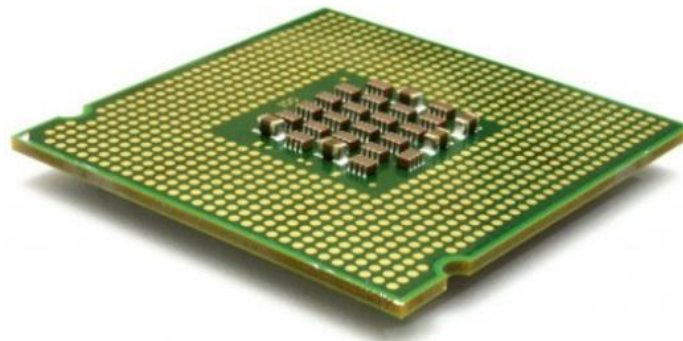


Figure 2: A Device Where the Adjustment of the “Cruising Height” Would be Critical to Avoid Hitting the Components in the Center of the Grid during Movement from Pin to Pin

4.4 Pogo Pin Tips (Round Versus Concave Versus Sharp)

The field induced waveform occurs as an air discharge, small changes in the discharge pogo pin's geometry can cause the waveforms to no longer meet the specification when performing waveform verification on the calibration targets. Although the standard does not specify using a round pogo pin, waveform parameters are based on this pogo shape. Unlike a round pogo tip, a pointed (sharp) tip changes the fields between the tip and the target and can adversely affect the waveform. Like a concave tip that may align better with a certain device pin shape, other shapes may also change the field when contacting pins of a device and subsequently change the waveform parameters.

Although device pins (contacts) have different shapes, the use of a round pogo tip keeps the electric fields more constant than a pointed or even a smaller diameter round tip. A typical standard pogo diameter is ~0.50 mm to 0.56 mm, and smaller diameters are ~0.38 mm to 0.44 mm. Full waveform verification should be done any time the pogo pin is replaced, but this is especially important if the pogo pin shape changes.

4.5 Humidity

Field induced waveforms occur as an air discharge and can be affected by many different factors, like the speed of approach, pogo tip shape, and the environment, or more precisely, the humidity levels within the test area (chamber). As humidity increases, amplitude drops, making testing at high humidity levels less stringent of a test. In addition to amplitudes being affected by humidity, repeatability is also affected by humidity levels, which are known to worsen as voltage levels decrease [1]. Although the standard specifies humidity should be less than 30% during testing and waveform verification, it is advisable to bring this level as low as possible using dry air or nitrogen brought directly into the test chamber. A small humidity meter placed inside the system can help determine the proper soak time for the desired humidity target level.

4.6 Cable Connections

The standard specifies the use of high bandwidth cables and components (connectors and attenuators) to ensure the best waveform performance and measurement integrity. For 6 GHz measurements, attenuators with a bandwidth of at least 12 GHz are recommended. The use of higher bandwidth components during all measurements further ensures measurement integrity.

Each added connector connection can introduce reflections on the discharge waveforms. For this reason, it is important to limit the number of connections and ensure the connections are tight using a torque wrench that uses the necessary force required to ensure the connections are tight without damaging the connectors. Most systems use SMA connectors, and torque wrenches are available for these connector types.

4.7 1-Ohm Current Sensing Resistance Measurements

The 1-ohm current sensing resistor is part of the discharge chain when performing CDM testing. Therefore, the resistance value must be correctly measured and known to compensate for peak current offset or to detect resistor degradation, which leads to changes in the shape of the discharge pulse.

Two-probe digital multimeters are not accurate enough to measure the 1-ohm current sensing resistor with an accuracy of 0.01 ohm (ANSI/ESDA/JEDEC JS-002, per Section 5.5 standard); therefore, Kelvin 4-wire connections should be used. Using Kelvin 4-wire connections, the current is supplied via a pair of force connections (Force High (FH) and Force Low (FL)) while the sensing pair (Sense High (SH) and Sense Low (SL)) connections measure the voltage across the resistor. The advantage of using the Kelvin 4-wire approach is that the voltage drop in the sense pair is negligible compared to the force pair, making a low ohmic resistance measurement. Figures 3a and 3b show the set-up for the 1-ohm current sensing resistance measurement using a Kelvin 4-wire approach. The 1-ohm current sensing resistor should either be terminated by the 50-ohm input of an oscilloscope or by a 50-ohm termination.

The following items should be taken into consideration to maximize the accuracy of the 1-ohm current sensing resistor measurement:

- Use of the maximum number of digits
- Slowest AC filter to increase accuracy
- The highest range for the number of power line cycles to increase accuracy
- Offset compensation to reduce or eliminates thermal electromotive force
- Warm-up time according to the resistance meter manual
- Measurement range (lower current ranges minimize self-heating of the 1-ohm current sensing resistor, but higher current ranges improve the accuracy of the measurement)

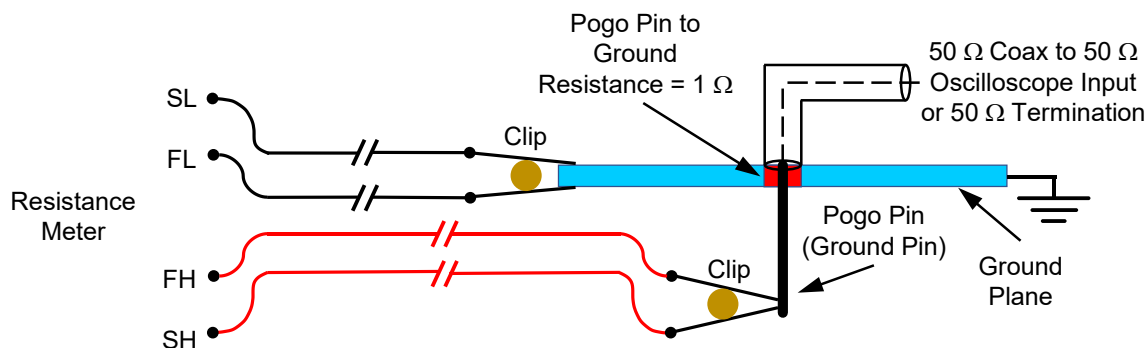


Figure 3a: Kelvin 4-Wire Resistance Measurement 1-Ohm Current Sensing Resistor Setup

NOTE: SL – Sense Low connection, SH – Sense High connection, FL – Force Low connection, FH – Force High connection



Figure 3b: Connection of the Kelvin 4-Wire Clips to the 1-Ohm Current Sensing Resistor Setup

Figure 4 shows the measurement accuracy influence for different types of ohmmeters versus applied current for two types of source measurement units (SMU, Keithley 2400 and 2450 – note equivalents are acceptable), a 6½ digit bench multimeter (Keysight 33401A or equivalent), and two handheld multimeters (Metra Hit/27M and Fluke 289 or equivalent). For the calculation, the specified measurement accuracy (\pm (% of reading + % of full scale) expressed in ohms) for each type of ohmmeter has been calculated for the 1-ohm resistor measurement. Using a Keysight 33401A bench multimeter, the best accuracy is obtained with the lowest applied measurement current and minimizing the risk of self-heating of the 1-ohm current sensing resistor during the measurement, see Figure 4. The same accuracy can also be obtained with one of the SMU's when the current is increased by a factor of 100 compared to the Keysight 33401A bench multimeter with the risk of self-heating.

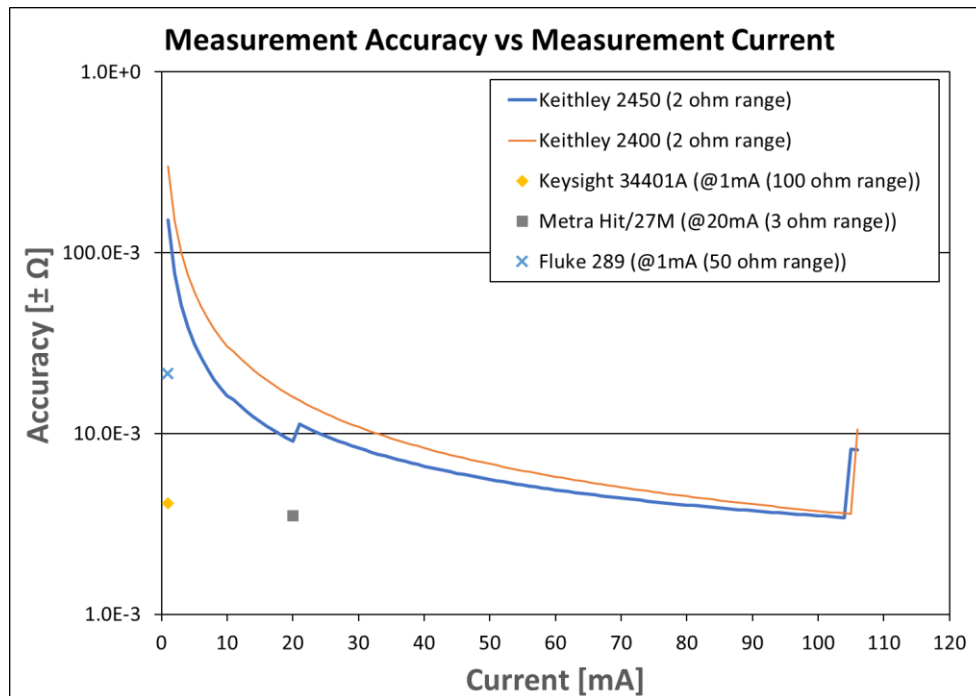


Figure 4: Calculated Measurement Accuracy Versus Measurement Current for Different Types of Ohmmeters When Measuring a 1-Ohm Current Sensing Resistor

NOTE: The Keysight 34401A, Metra Hit/27M, and Fluke 289 have a fixed range measuring a 1-ohm resistor.

NOTE: Accuracy is improved with lower readings on the above Y-axis – ideally, the measurement accuracy of less than 10^{-3} ohm is desired.

NOTE: Measurement accuracy = \pm (% of reading + % of full scale) expressed in ohms.

5.0 OSCILLOSCOPE EFFECTS - SETTINGS

5.1 Metrology Concerns

Four metrology considerations need to be understood when setting up to capture and analyze CDM waveforms.

- Proper cabling and attenuator selection
- Proper oscilloscope selection
- Oscilloscope variation concerns
- Proper data capture and analysis

5.2 Proper Cabling and Attenuator Selection

Due to the nature of the CDM waveforms, with very fast rise times and short durations, all the items within the metrology chain must be of good quality and have the proper bandwidth to minimize questions or concerns during waveform verification or actual device testing.

Cables, attenuators, and bandwidth filters should be chosen to meet the calibration requirements of ANSI/ESDA/JEDEC JS-002, which means they should have a minimum bandwidth of at least 12 GHz. However, it is advisable to have even higher bandwidths to provide the best accuracy. Many of today's SMA coax cables and attenuators are available with a bandwidth of 18 GHz.

An important item within the metrology chain is the coax connectors and adapters being used. High quality, high bandwidth connectors/adapters, preferably SMA style, should be used. It is also very important that "all" connections be tight to avoid any noise or reflection issues caused by a bad connection.

5.3 Oscilloscope Variation Concerns

There are many reasons why waveform variations can occur between oscilloscopes with different bandwidths or even oscilloscopes with the same bandwidth when measurements are made at or near the high end of the oscilloscope's bandwidth. Oscilloscopes with bandwidth specifications greater than 1 GHz typically have a maximally-flat frequency response, but there are different techniques manufacturers can use to achieve the result [2][3].

Figure 5 shows high bandwidth oscilloscope frequency responses for three different manufacturers; although they are well above the suggested frequency for CDM waveform capture the same considerations apply in the 6-GHz range.

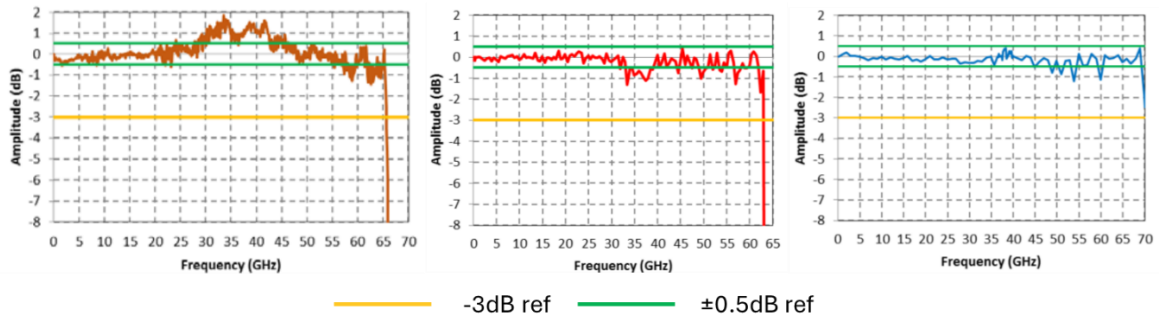


Figure 5: Frequency Response for High Bandwidth Oscilloscope

Using maximally flat response generally provides accurate measurements when signals are within the oscilloscope's bandwidth; however, this is not always the case since these may not have a very flat frequency response and might be 1 to 2 dB up or down in the region of interest for the waveform being measured. A 1-dB low response on any oscilloscope would mean an error in measurement of approximately 10.9%.

Another issue to be aware of is that some modern oscilloscopes specify a minimum bandwidth, which means an oscilloscope specified at 6 GHz, may actually have a bandwidth of 6.1 GHz or 6.2 GHz. To further complicate matters, the bandwidth sometimes changes depending on the vertical setting of the oscilloscope.

5.4 Proper Data Capture and Analysis

The current sensor is a 1-ohm resistor in parallel with a 50-ohm cable connected to the oscilloscope. The resistor itself is allowed to be 10% higher or lower than the target value. Therefore, it is important to consider the actual resistor value when determining the waveform's true peak current from the oscilloscope readings. The oscilloscope capture points should be corrected by dividing them by the parallel between 50 ohms and the real resistance value measured as suggested in Section 4.7.

Oscilloscope sample rate plays a fundamental role in data analysis; commercially available 6-GHz oscilloscope sample rates range from 20 Gs/s to 60 Gs/s. A 20-Gs/s sample rate describes a 200-ps rise time waveform with a maximum of four points; this reduced rise time resolution may affect the minimum value of the acquired rise time, making the waveform parameter analysis more difficult.

Another consideration should be done on vertical scale settings. High-speed digital oscilloscopes usually have a limited resolution, typically eight bits in the single-shot mode used during CDM waveform capture. It is important to adjust the measurement range and offset of the oscilloscope to best use the available resolution. The gain and offset controls should be chosen to obtain close to a full-scale waveform without clipping the waveform. However, the use of "fine vertical scale" should be avoided because this adjustment may create a better-looking waveform on the screen but does not improve the measurement resolution.

Correct attenuator choice is also fundamental for low voltage stress and tiny ICs: a small vertical scale is generally noisier than the others and should be used only when needed. Attenuator choice should consider the maximum input voltage to avoid damage on the first input stage.

6.0 DETERMINING IF A CHARGE TIME (DELAY) IS NEEDED

With larger packaged units, it may be necessary to add additional charge time (delay) into the CDM tester to ensure the product under test received a full charge before discharge. This typically starts to become an issue when the package size exceeds 500 mm² when a charging resistor of approximately 100 megohms is installed but can also occur at lower package sizes if this charging resistor is larger. It is recommended that each new large package (> 500 mm²) tested on a CDM tester for the first time go through this procedure to ensure the delay has been set properly.

NOTE: Charge time (delay) is the amount of time the device is allowed to charge – any added time is added to the default in most cases.

NOTE: Discharge time (delay) is the amount of time that the pogo pin remains in contact with the pin under test – any added time is added to the default in most cases.

6.1 Procedure for Determining if a Charge Time (Delay) is Needed

The procedure below can be used to determine if a charging delay is needed. It is recommended to run this evaluation using a primary GND or VSS pin on the package.

1. Set the field plate voltage at +250 volts. Any voltage can be used as the objective is to monitor the peak current (I_p). However, voltages lower than 250 volts should be avoided due to I_p stability, and higher voltages should only be used if the product can tolerate it without being damaged.
2. With the charge time (delay) set to 0 ms, collect ten waveforms and record the I_p from each. Calculate the average I_p of the waveforms.
3. With the charge time set to 500 ms, collect ten waveforms, record the I_p from each. Calculate the average I_p of the waveforms.
4. Compare the average I_p value from the charge time of 0 ms and the charge time measurement at 500 ms. If the average I_p for the charge time of 0 ms is at least 95% of the average I_p for the charge time of 500 ms, then the package to be tested has a capacitance small enough not to require an added delay. If the average I_p for the charge time of 0 ms is less than 95% of the average I_p for the charge time of 500 ms, refer to the procedure below to determine the appropriate charge time to ensure the device receives a full charge.

The procedure below can be used for characterizing the charge time on the CDM tester and determining the appropriate charge time (delay) for full charging. The below procedure is used if step 4 above determines that the I_p value does not align between the 0 ms and 500 ms comparison.

6.2 Procedure for Setting Charge Time (Delay)

Typically, the primary GND or VSS bus of a product is reasonably robust when zapped at + 250 volts and can be used as a good reference point when setting up for this procedure. However, any pin can be used that the user believes would not be damaged by the discharge at the set voltage. The below procedure's objective is to characterize the I_p at various charge time points, focusing on looking for a point where the I_p saturates (no longer increases in value). The charge time setting corresponding to the point at which the I_p saturates would be the minimum delay that should be set. It is recommended to be conservative and add 50 ms to 100 ms to the determined delay value.

Follow the procedure below, using the identified pin on the package under consideration, to determine an appropriate charge time (delay):

1. Set the field plate voltage at + 250 volts (any voltage can be used as the objective is to monitor I_p).

2. With the charge time (delay) set to 0 ms, collect ten waveforms and record the I_p from each. Calculate the average I_p of the waveforms.
3. Increase the charge time (delay) by 50 ms, collect ten waveforms, record the I_p from each, and calculate the average I_p .
4. Continue incrementing the charge time by 50 ms (a larger or smaller step can be chosen) and record the average I_p until a minimum of 500 ms charge delay.
5. Plot the results, as shown below in Figure 6.
6. The appropriate charge time (delay) results in a “saturation point” for the I_p . As shown below in Figure 6, the I_p for this example saturates at just over 5.4 amperes at 300 ms. Adding some guardband to this example would set a charge time (delay) of 350 ms – 400 ms as the required charge time (delay) on this example package device.
7. It is expected that 500 ms or less is sufficient to reach a saturation point for most large devices. However, if after 500 ms, a saturation point has not been reached, repeat steps 4 & 5 until this occurs.
8. It is important to note that longer charge times do not “overcharge” the device but would only increase test time, so balancing charge time (delay) is important to minimize the overall test time.

NOTE: To avoid the risk of not fully discharging the device, it is a good practice to set the discharge time (delay) to align with whatever charge time (delay) was determined in the above procedure.

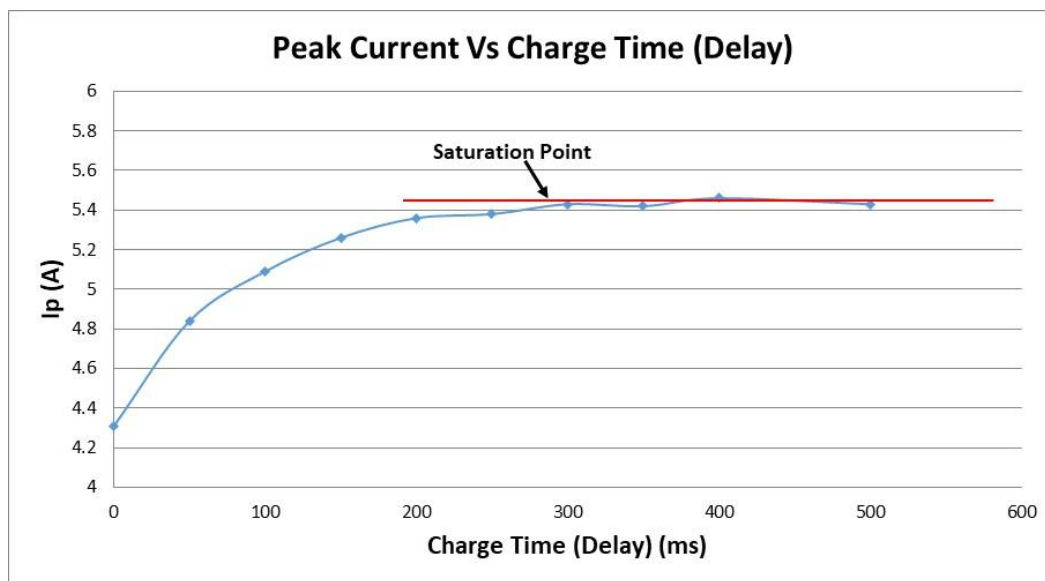


Figure 6: Example Characterization of Charge Time (Delay) Versus I_p

7.0 WAVEFORM VERIFICATION PROCEDURE – FACTOR/OFFSET

7.1 Factor/Offset Adjustment Method

This procedure aligns the tester for direct software voltage input of the Test Condition (TC) for the full alignment range. This method may not allow for alignment of each Test Condition with the target mid-range of I_p , as shown in Table 1 of ANSI/ESDA/JEDEC JS-002. However, it is the easiest to use in a lab environment with multiple testers because the software voltage entered matches the Test Condition target level. It also does not require linear interpolation/extrapolation for Test Conditions other than the five levels listed in Table 1 of ANSI/ESDA/JEDEC JS-002.

Using the factor/offset feature available on many CDM testers adjusts the field plate voltage based on the software's target voltage (software voltage). This adjustment allows a user to always enter the Test Condition target with the system adjusting the field plate voltage to hit the target I_p .

The requirements/details of this factor/offset adjustment method are as follows:

- A single factor/offset is used across the entire Test Condition range. In other words, the user must determine a single factor/offset value that can be used across the full set of TCs, which typically means there is some compromise with trying to hit the mid-point of the range across all 5 TCs.
- A different factor/offset can be used for each polarity. Most CDM test systems allow a separate adjustment for positive and negative voltages, typically the same value for factor/offset can be used for both polarities, but both polarities must be checked.
- The same factor/offset must be used for both large and small verification modules.

The pros/cons of this approach are listed below:

- Pros
 - Easiest to use in a lab with many testers as the target TC voltage is entered in the user's software. Therefore, the system user can avoid determining unique field plate voltages values to enter for each TC but can enter the target voltage aligned with each TC (for example, entering a software voltage of 250 volts for TC 250).
- Cons
 - I_p may not align to the center of the I_p range for each Test Condition. Since a fixed factor/offset must be used across all 5 TCs, it is typically expected that the user does not achieve the mid-point of the target range for every TC. This could be done, but the effort required would not make the use of this approach very practical.

Figure 7 shows the full qualification or quarterly flow check required to follow the requirements specified in ANSI/ESDA/JEDEC JS-002. This section of the user guide steps the user through this flow, step by step, to help better understand what is expected of the user. Note that while the flow in Figure 7 shows completing the large or small verification module first, then completing the other, any combination of checking the large and small verification module is acceptable as long as all TCs are completed for both verification modules and the requirements listed previously for this adjustment method are met.

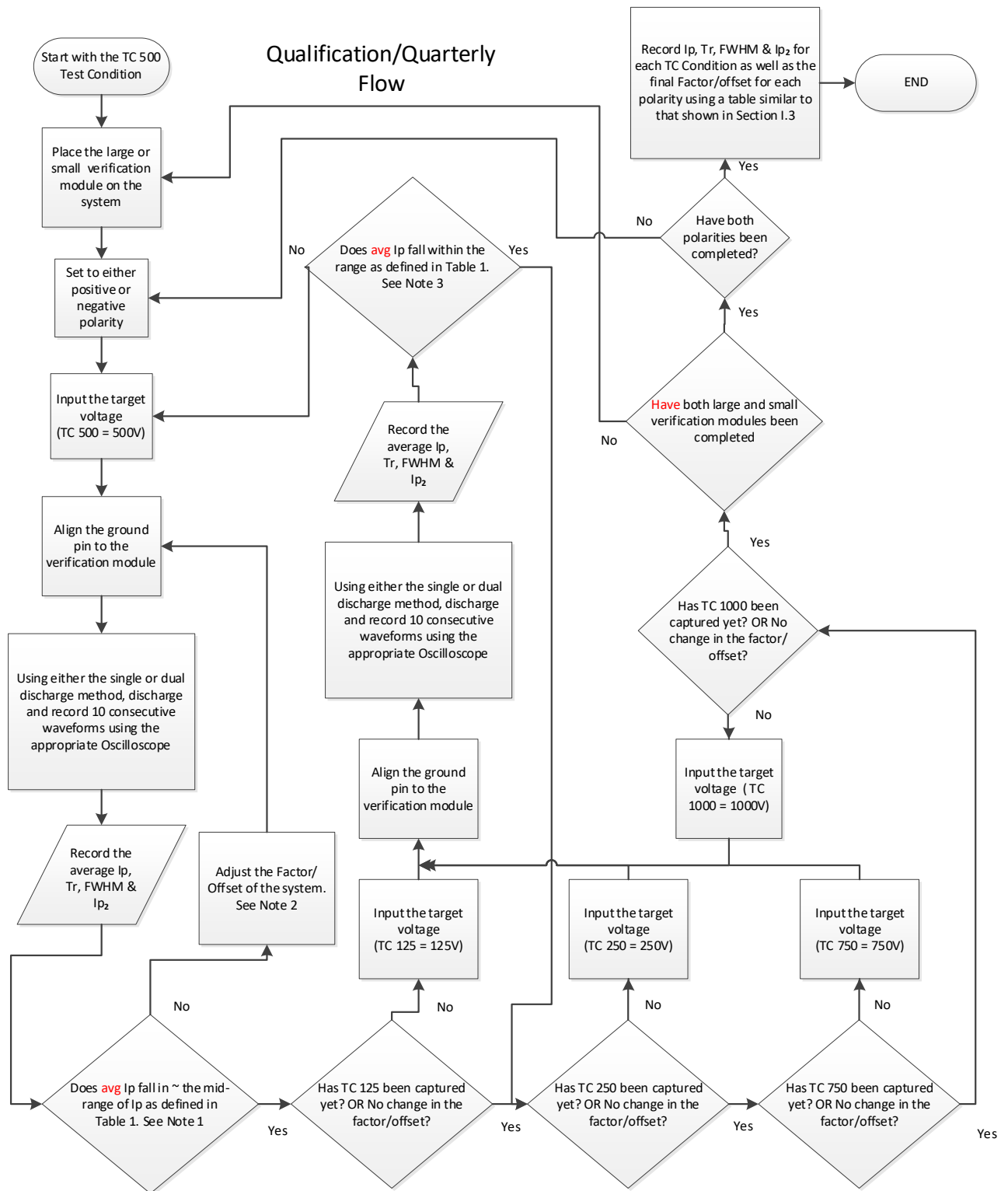


Figure 7: Example Waveform Verification Flow for Qualification and Quarterly Checks Using the Factor/Offset Adjustment Method

NOTE 1: Targeting the mid-range of TC 500 is a starting point for adjusting the field plate voltage. Based on the results of the other Test Conditions (TC 125/250/750/1000), the I_p may end up higher or lower than the mid-range value on TC 500. Adjustments in the factor/offset may shift the I_p higher or lower, as shown in Figures 8 and 9.

NOTE 2: To properly calibrate systems, tester manufacturers have implemented a secondary “adjustment” parameter as an offset from the software voltage setting, either represented as a voltage “multiplier” value or a percentage “offset” value, which modifies the field plate voltage. Consult the tester manufacturer for more detail.

NOTE 3: After several iterations through this loop, if the user finds they cannot meet the I_p range as defined in Table 1 of ANSI/ESDA/JEDEC JS-002, or the factor/offset is outside the typical documented range, re-clean the verification modules and pogo pin and check that all connections are tight. If this still does not work, check the system vacuum, or replace the pogo pin. Consult the tester manufacturer for more information.

7.2 Factor/Offset Adjustment Impacts

Before proceeding into the verification process detail, it is necessary to review some background on how the factor or offset impacts the shape of the I_p curve as a function of the voltage setting. The actual field plate voltage is modified by multiplying the factor by the software voltage setting by adjusting the factor. For example, a software voltage setting of 500 volts would result in a field plate voltage of 450 volts with a factor of 0.9. As shown in Figure 8, the center curve (in red) depicts a typical I_p versus software voltage setting. If we assume the center curve depicts a situation in which the factor equals one, as the factor is adjusted lower, the actual slope of the I_p versus software voltage curve becomes shallower.

Consequently, as the factor is adjusted higher, the slope of the I_p versus software voltage curve becomes steeper. Adjusting the factor is the most typical way to ensure meeting the target levels.

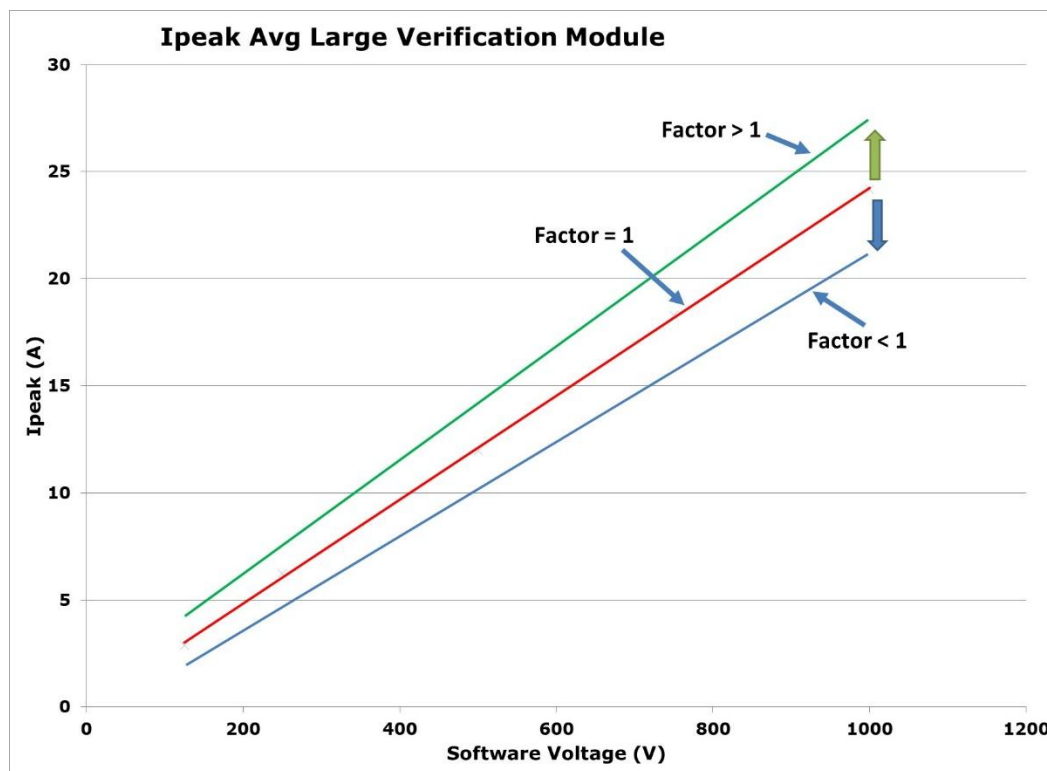


Figure 8: Example of the Impact of Factor Adjustment on the Average I_p for the Large Verification Module

Additionally, some CDM ESD testers offer a second way to adjust the I_p versus voltage curve. This is known as the offset. By adjusting the offset, the actual field plate voltage is modified by adding the offset to the software voltage setting. For example, a software voltage setting of 500 volts would result in a field plate voltage of 450 volts with an offset of -50 volts. Note that the offset can be either a positive or negative value. As shown in Figure 9, the center curve (in red) depicts a typical I_p versus software voltage setting. If we assume the center curve depicts a situation in which the offset equals zero, as the offset is set below zero, the actual curve of the I_p versus software voltage curve is lowered with no change in the slope. Consequently, as the offset is increased above zero, the I_p versus software voltage curve is raised with no change in the slope. Adjusting the offset can be used for finer adjustments and can help meet the TC 125 condition's tighter range. Note that if offset is used to make adjustments at higher Test Conditions, it does pose a risk of creating too large an adjustment for TC 125 and lower Test Condition settings.

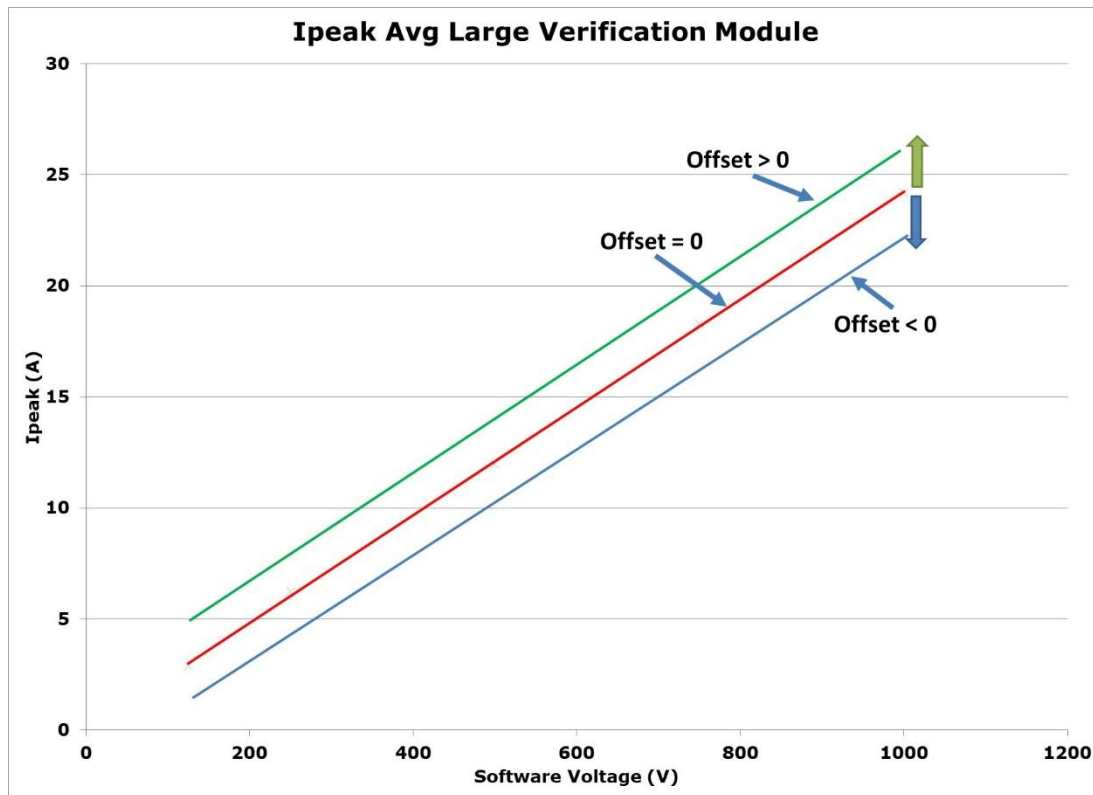


Figure 9: Example of the Impact of Offset Adjustment on the Average I_p for the Large Verification Module

7.3 Factor/Offset Adjustment Method Details

7.3.1 Positive Polarity Waveform Verification

Figure 10 breaks out the first leg of the flow chart shown in Figure 7 and focuses on just the first check at TC 500. The check can start with any TC, and experience on a CDM tester may find that a different TC is best to start with (for example, starting with the TCs most often used for product qualifications and ensuring these are best aligned to the center of the target range). However, for this example, the user guide follows the flow shown in Figure 7 and starts with TC 500.

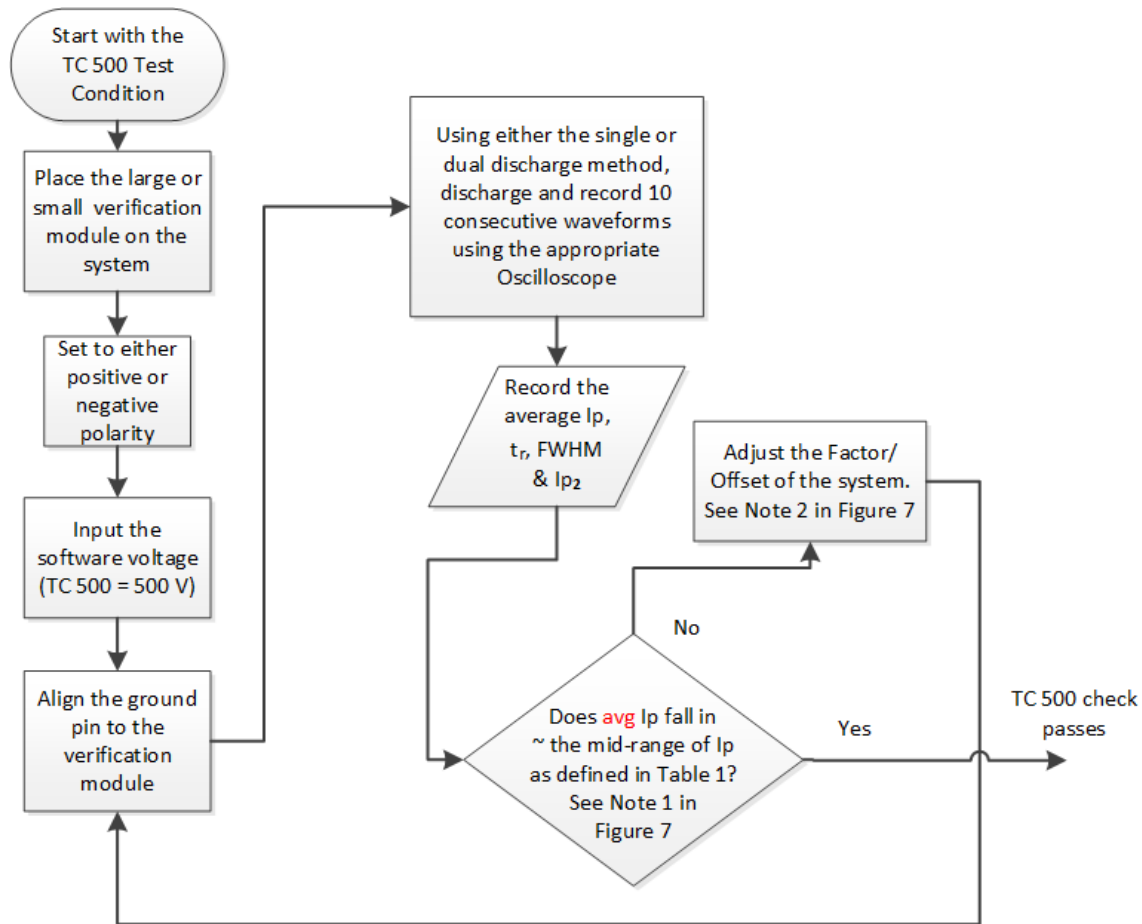


Figure 10: Example of the TC 500 Verification Flow for Qualification and Quarterly Checks Using the Factor/Offset Adjustment Method

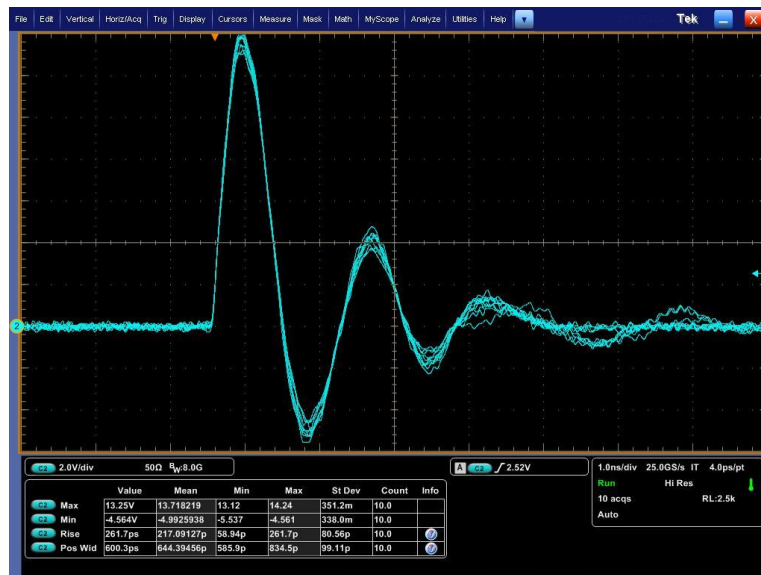
The objective in the first step is to adjust the factor/offset to align the TC 500 setting to the mid-point of the target range, as shown in Table 1 of ANSI/ESDA/JEDEC JS-002. This sets up the best situation for getting alignment of the other TC conditions, which are checked afterward. It should be noted that all examples shown in this user guide are based on Table 1 of JS-002, which is the single waveform parameter table required for all quarterly waveform checks, qualification and yearly re-qualification checks. Table 1 is copied here just for ease of reference. Please see the note after Table 1 regarding the interpretation of t_r (rise time) of the waveform.

Table 1 of ANSI/ESDA/JEDEC JS-002 (Copied here for ease of reference)

		Test Condition									
		TC 125		TC 250		TC 500		TC 750		TC 1000	
Verification Module	Sym.	Small	Large	Small	Large	Small	Large	Small	Large	Small	Large
Peak Current (amperes)	I_p	1.4-2.3	2.3-3.8	2.9-4.3	4.8-7.3	6.1-8.3	10.3-13.9	9.2-12.4	15.5-20.9	12.2-16.5	20.6-27.9
Rise time (ps)	t_r	<250	<350	<250	<350	<250	<350	<250	<350	<250	<350
Full width at half maximum (ps)	FWHM	250-600	450-900	250-600	450-900	250-600	450-900	250-600	450-900	250-600	450-900
Undershoot (A, max. 2nd peak)	I_{p2}	<70 % I_p	<50% I_p	<70 % I_p	<50% I_p	<70 % I_p	<50% I_p	<70 % I_p	<50% I_p	<70 % I_p	<50% I_p

NOTE: t_r also refers to the similar first peak transition time to a negative maximum for the negative going CDM first peak pulse.

Figure 11 shows an example of the first set of 10 waveforms captured when collecting the TC 500 condition on the large verification module. Figure 11 shows the raw voltage measurements and must be adjusted for the correct resistance in the discharge head ($I = V/R$). For all the examples shown in this section, the resistance of the discharge head is 1.03 ohms.

**Figure 11: Initial Large Verification Module Reading at TC 500**

As can be seen, the initial I_p is a little on the high side, running at an average value of 13.3 amperes ($I = 13.7 \text{ volts}/1.03 \text{ ohms}$) for the average of the ten waveforms compared to a target of ~12.1 amperes. It should be noted here that not all ten waveforms must be within specifications,

but the average must be. The reading is not expected to be exactly 12.1 amperes, but the value of 13.3 amperes is a little on the high side. In this case, it is prudent to adjust the factor and align closer to 12.1 amperes. This ensures a higher success of meeting the requirements across all the Test Conditions without additional adjustments. Typically, the factor is used as the primary adjustment method. The offset can be considered as the “fine” adjustment. If the offset is being adjusted, it is typically because of an adjustment needed at TC 125. But in most cases, the offset remains at 0.

Figure 12 shows the result after a decrease in the factor. In this case, the average I_p is now 12.6 amperes ($I = 12.95 \text{ volts}/1.03 \text{ ohms}$).

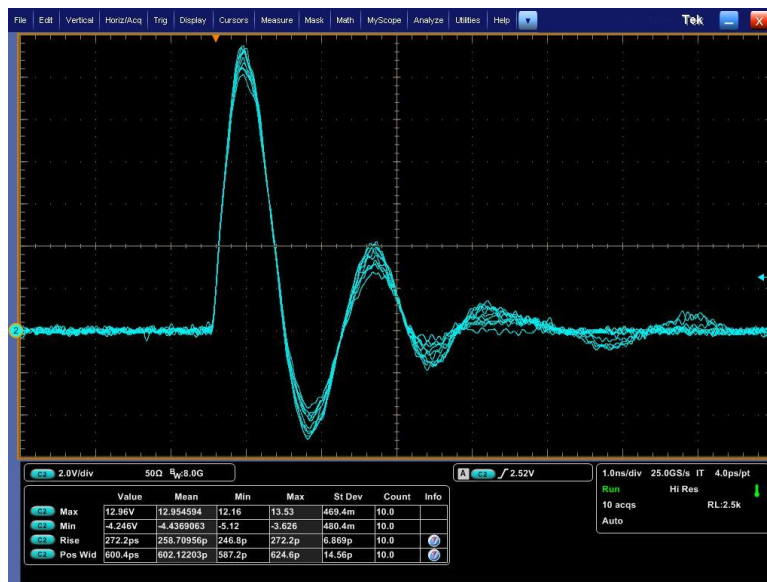


Figure 12: Large Verification Module Reading at TC 500 After Initial Factor Adjustment

A final I_p of 12.1 amperes is achieved ($I = 12.47 \text{ volts}/1.03 \text{ ohms}$) with one more decrease in the factor, as shown in Figure 13. More than close enough to start checking other TC conditions. For this example, a factor of 0.82 with an offset of 0 volt was determined for the positive waveforms' final settings. It should be noted that the final factor adjustment shown in Figure 13 was not as critical and that the factor/offset used to get the waveforms in Figure 12 would have been just fine.

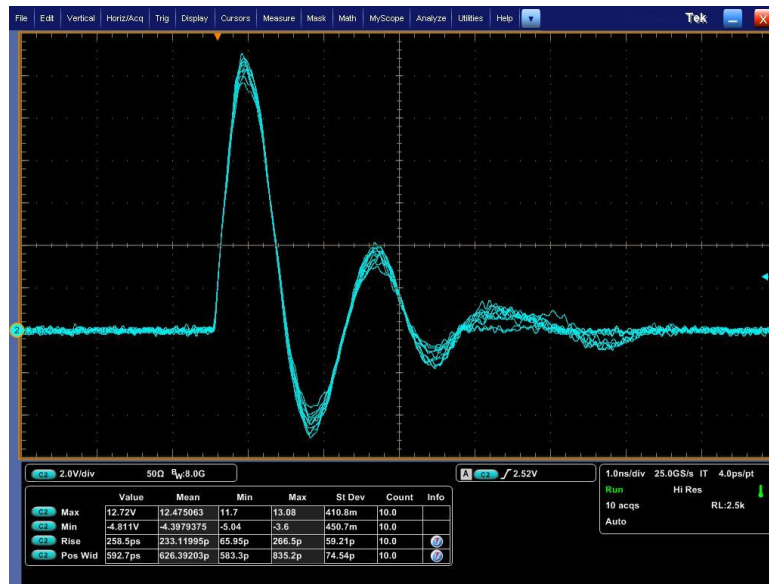


Figure 13: Large Verification Module Reading at TC 500 After Final Factor Adjustment

According to Figure 7, the next step in the flow would be to check the large verification module at all other TC conditions, starting with TC 125 (see Figure 15). As shown in the flow, if any change in the factor or offset is required as a result of not meeting the requirements at TC 125 (or any other TC check after TC 500), then the user must go back and recheck the TC 500 condition (and any other TC condition that may have been completed). There are a couple of options here for how to proceed:

- One option is to follow the flow as defined and check the large verification module at the other TC conditions. This can be done very quickly and does not require any additional alignment checks on the system.
- A second option here is to check the small verification module at TC 500 before moving on to the TC 125 check. This does require some extra work at TC 500 before moving on but can be valuable in saving time overall by limiting any need to adjust factor/offset later on in the overall flow, as called out in Figure 7.

There is no clear best option between the two, and experience helps the user decide which option is best for the system under test.

With that in mind, Figure 14 shows a quick check of the small verification module at TC 500 before moving on to the TC 125 check. The I_p shown is 7.2 amperes ($I = 7.4 \text{ volts}/1.03 \text{ ohms}$). Well within the target range, and with this reading, it was concluded that moving on to the TC 125 check makes sense.

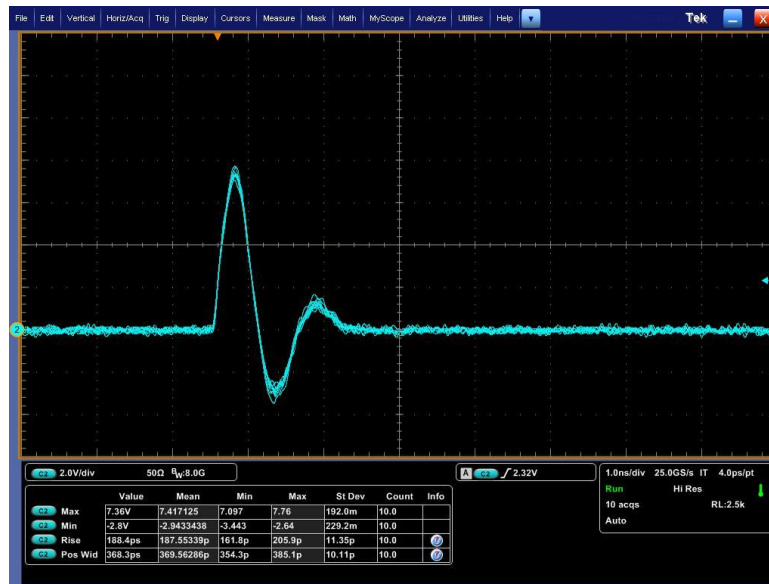


Figure 14: Small Verification Module Reading at TC 500 After Final Factor Adjustment

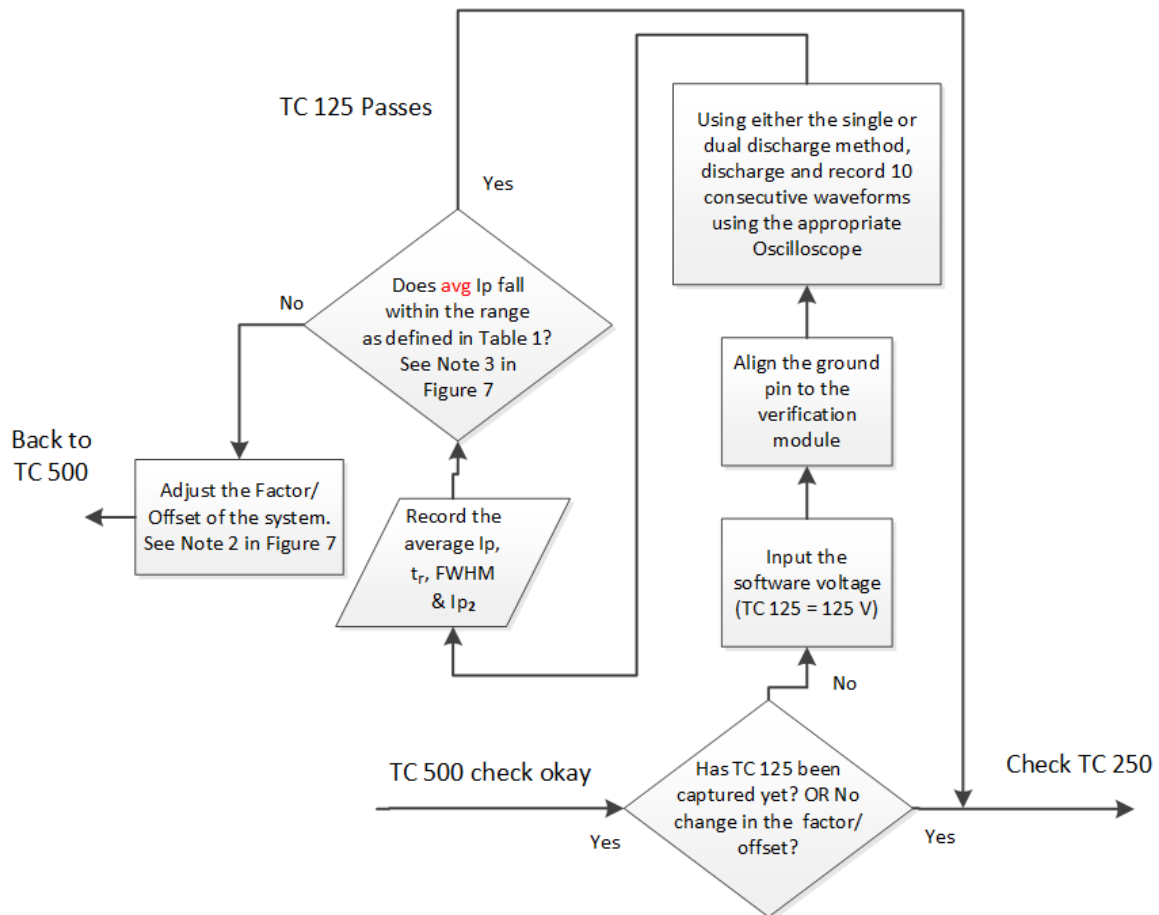


Figure 15: Example of the TC 125 Verification Flow for Qualification and Quarterly Checks Using the Factor/Offset Adjustment Method

Now that the TC 500 check was completed, the user can proceed with the check at TC 125 on the large verification module (see Figure 15). This example focuses on checking the large verification module first across the remaining four TCs (TC 125, 250, 750, and 1000) before checking the small verification module. However, it should be noted that either verification module could be checked first since both were checked and confirmed to be within specifications (as called out in Table 1 of ANSI/ESDA/JEDEC JS-002) at TC 500.

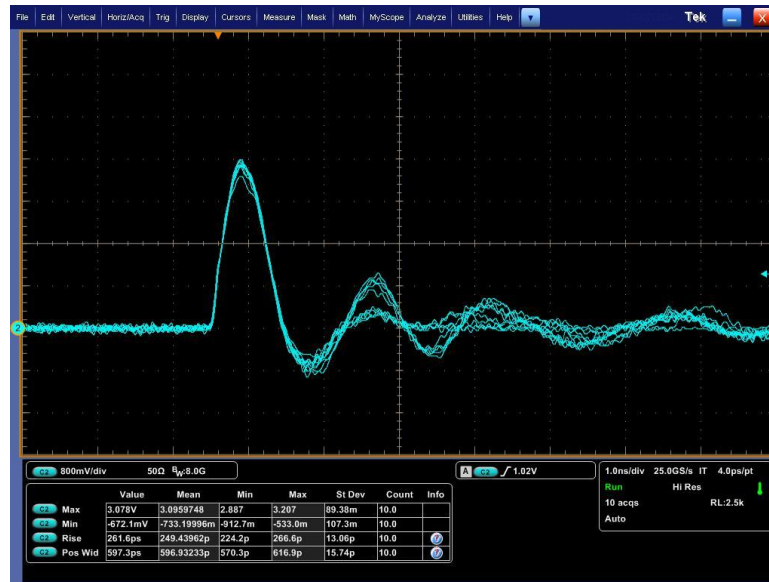


Figure 16: Large Verification Module Reading at TC 125

Figure 16 depicts the waveforms for TC 125 on the large verification module. The I_p reading for TC 125 is 3.0 amperes ($I = 3.1 \text{ volts}/1.03 \text{ ohms}$). This is well within the I_p target range, according to Table 1, and no factor/offset change is required. Now that the TC 125 check is completed for the large verification module, the TC 250 check can be completed for the large verification module according to the flow shown in Figure 17.

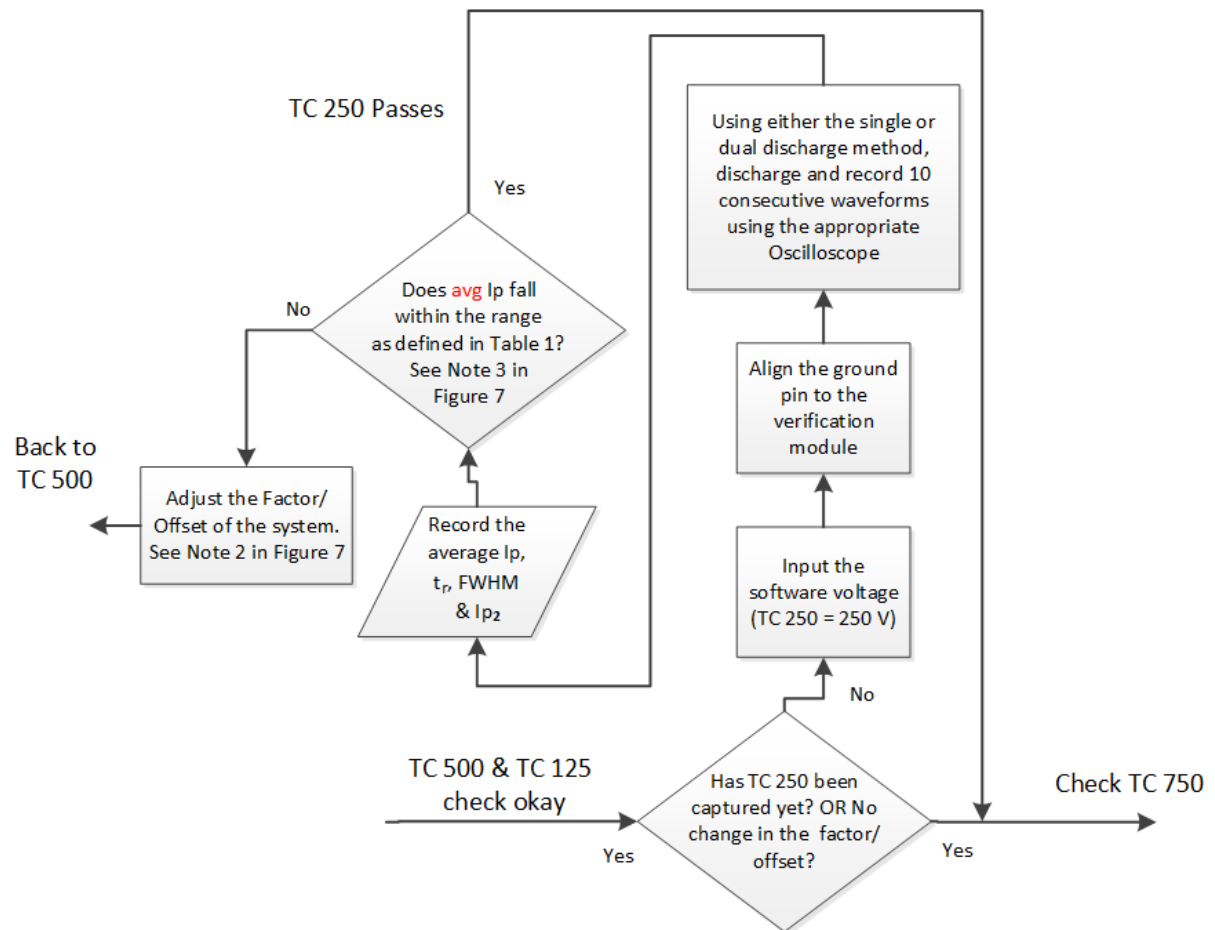


Figure 17: Example of the TC 250 Verification Flow for Qualification and Quarterly Checks Using the Factor/Offset Adjustment Method

The results of this check are shown in Figure 18. The I_p recorded from this run is 6.2 amperes ($I = 6.4$ volts/1.03 ohms). This is well within the target range for the large verification model at TC 250 according to Table 1 of ANSI/ESDA/JEDEC JS-002, and no factor/offset change is required, so the check now moves on to TC 750, as shown in Figure 19.

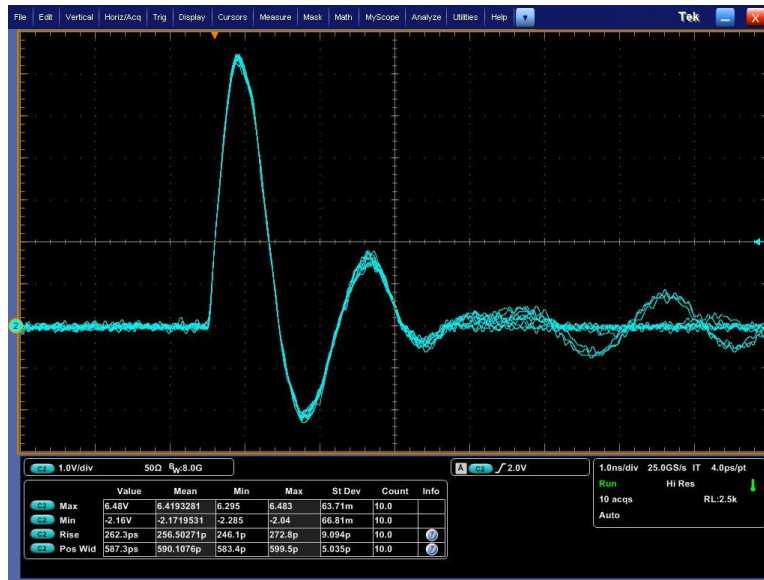


Figure 18: Large Verification Module Reading at TC 250

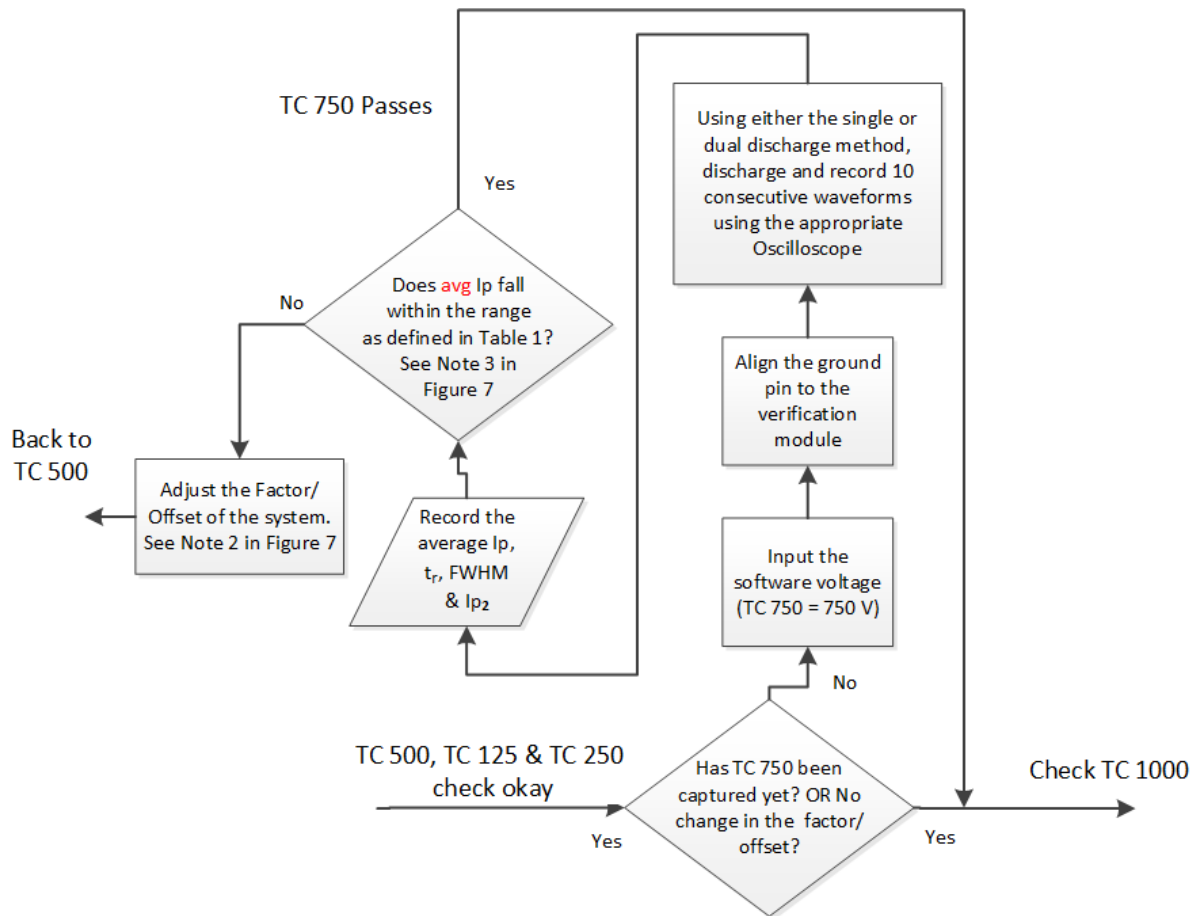


Figure 19: Example of the TC 750 Verification Flow for Qualification and Quarterly Checks Using the Factor/Offset Adjustment Method

The TC 750 check can be completed according to the flow shown in Figure 19. The results of this check are shown in Figure 20. The I_p recorded from this run is 17.8 amperes ($I = 18.4 \text{ volts}/1.03 \text{ ohms}$). This is well within the target range for the large verification model at TC 750 according to Table 1 of ANSI/ESDA/JEDEC JS-002, and no factor/offset change is required, so the check now moves on to TC 1000 check, as shown in Figure 21.

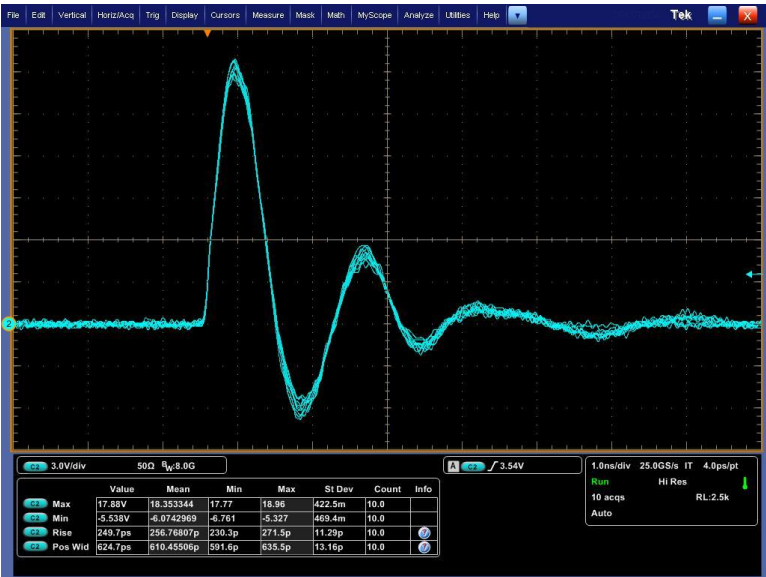


Figure 20: Large Verification Module Reading at TC 750

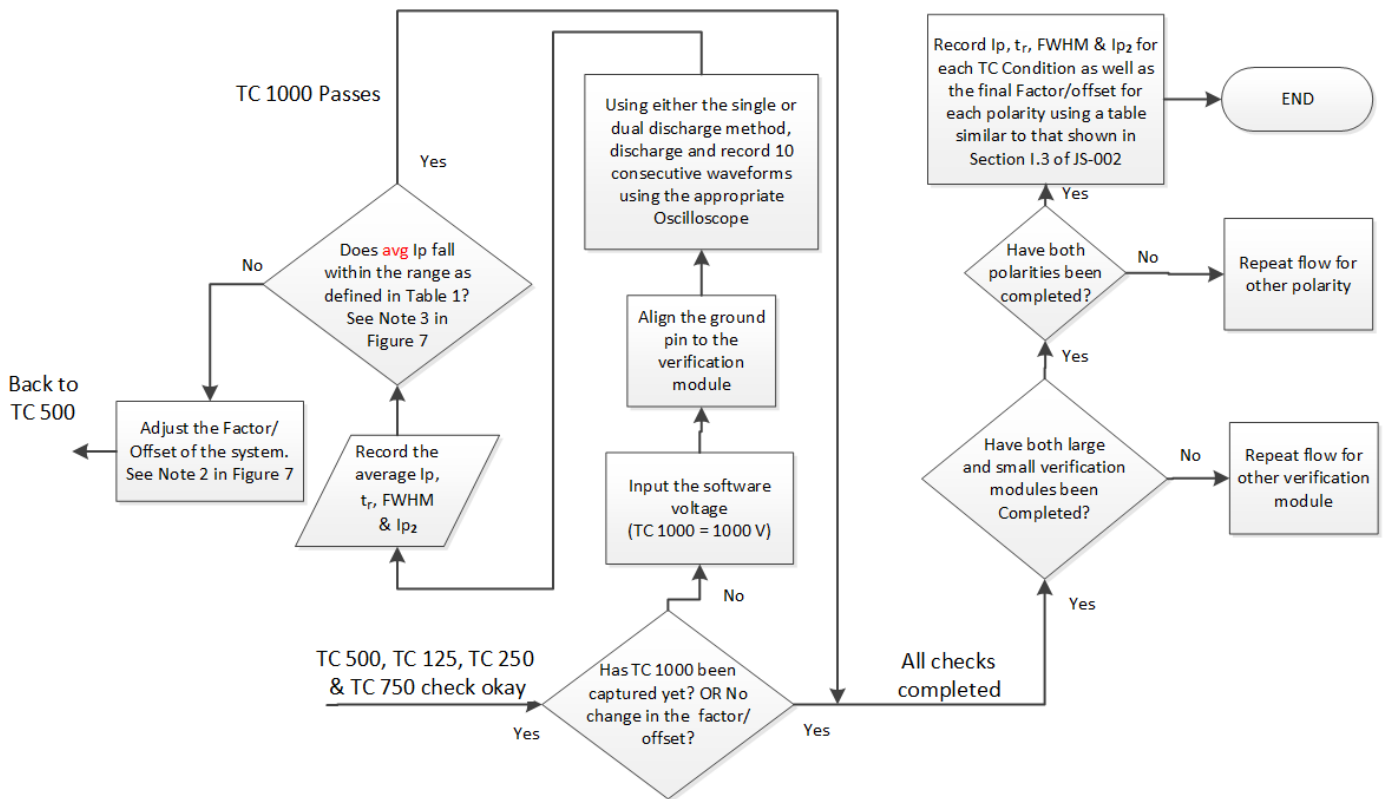


Figure 21: Example of the TC 1000 Verification Flow and Post TC 1000 Checks for Qualification and Quarterly Checks Using the Factor/Offset Adjustment Method

The results of the TC 1000 check are shown in Figure 22. The I_p recorded from this run is 24.2 amperes ($I = 24.9$ volts/1.03 ohms). This is well within the target range for the large verification model at TC 1000, according to Table 1 of ANSI/ESDA/JEDEC JS-002, and no factor/offset change is required. Now that the TC 1000 check is complete and all levels have passed for the large verification module, the next check is to verify the small verification module using the same factor/offset settings used for the large verification module in the positive polarity. The small verification module was already checked at TC 500. Figures 23, 24, 25, and 26 depict the results at TC 125, TC 250, TC 750, and TC 1000, respectively, for the small verification module. The results pass all the requirements in Table 1 of ANSI/ESDA/JEDEC JS-002, and no factor/offset change is needed.

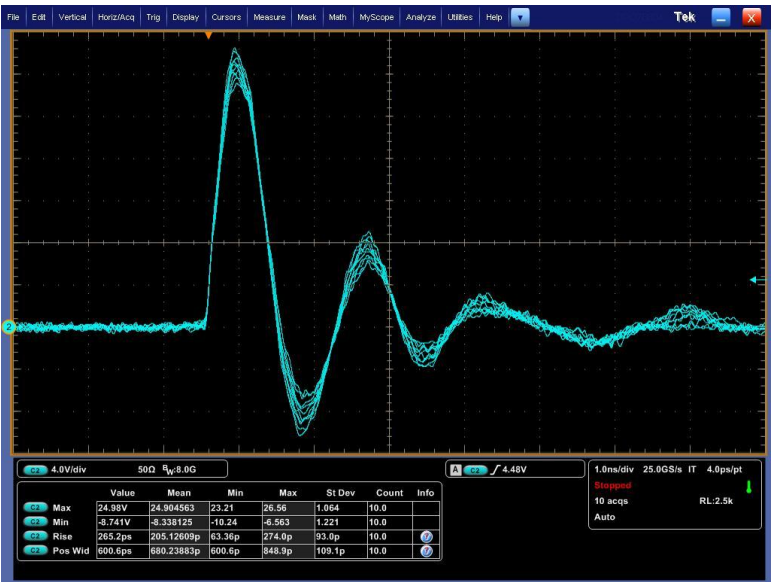


Figure 22: Large Verification Module Reading at TC 1000



Figure 23: Small Verification Module Reading at TC 125

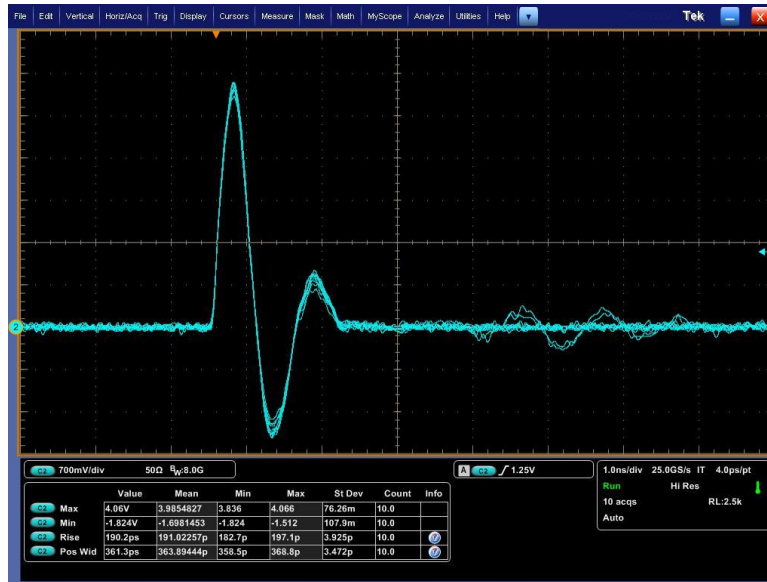


Figure 24: Small Verification Module Reading at TC 250

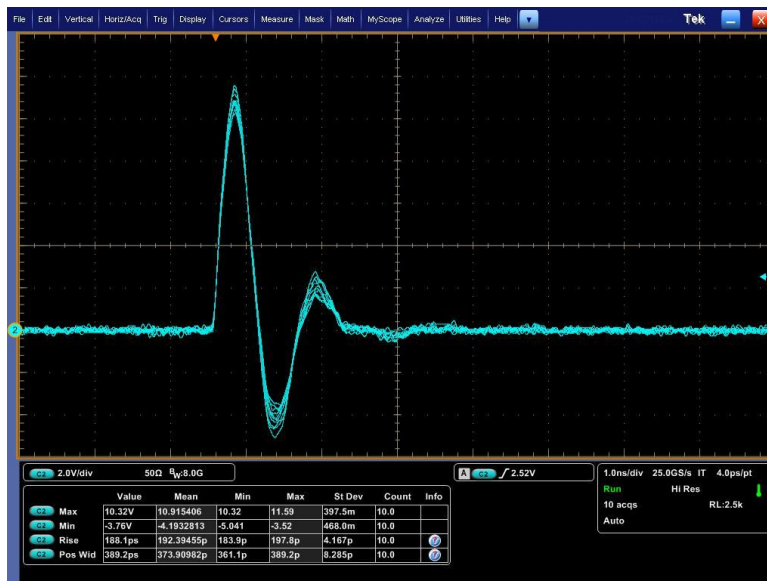


Figure 25: Small Verification Module Reading at TC 750

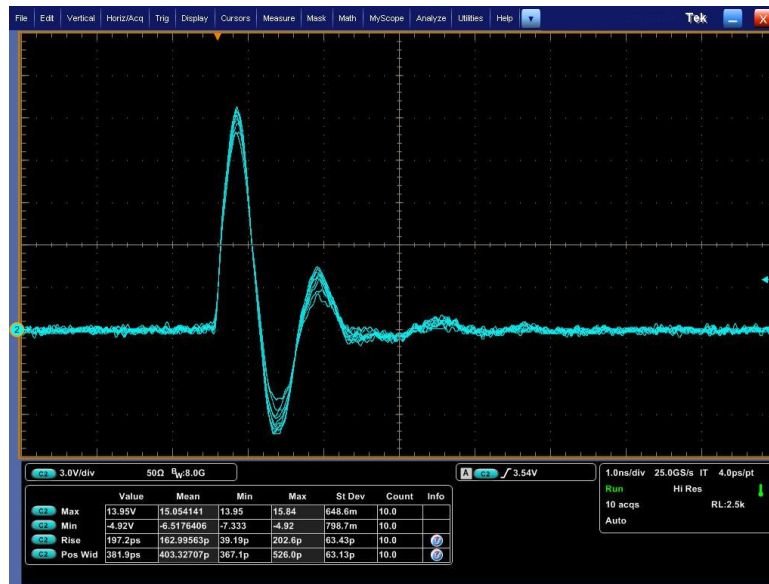


Figure 26: Small Verification Module Reading at TC 1000

In reviewing the small verification module, positive waveform results for each are shown in Table 1 (factor = 0.82/offset = 0 volts):

Table 1. Small Verification Module Positive Waveform Summary – Factor/Offset Adjustment Method

Test Condition	I _{peak}	t _r , FWHM and I _{p2}	Figure Reference
TC 125	1.75 amperes (I = 1.82 volts/1.03 ohms)	Pass	Figure 23
TC 250	3.9 amperes (I = 4.0 volts/1.03 ohms)	Pass	Figure 24
TC 500	7.2 amperes (I = 7.4 volts/1.03 ohms)	Pass	Figure 14
TC 750	10.6 amperes (I = 10.9 volts/1.03 ohms)	Pass	Figure 25
TC 1000	14.7 amperes (I = 15.1 volts/1.03 ohms)	Pass	Figure 26

In reviewing the large verification module, positive waveform results for each are shown in Table 2 (factor = 0.82/offset = 0 volts):

Table 2. Large Verification Module Positive Waveform Summary – Factor/Offset Adjustment Method

Test Condition	I _{peak}	t _r , FWHM and I _{p2}	Figure Reference
TC 125	3.0 amperes (I = 3.1 volts/1.03 ohms)	Pass	Figure 16
TC 250	6.2 amperes (I = 6.4 volts/1.03 ohms)	Pass	Figure 18
TC 500	12.1 amperes (I = 12.5 volts/1.03 ohms)	Pass	Figure 13
TC 750	17.8 amperes (I = 18.4 volts/1.03 ohms)	Pass	Figure 20
TC 1000	24.2 amperes (I = 24.9 volts/1.03 ohms)	Pass	Figure 22

It should be noted here that while ANSI/ESDA/JEDEC JS-002 only shows t_r in Table 1, the implication is that the requirement applies to checking negative waveforms also.

7.3.2 Repeat with Negative Polarity

According to the flow, as shown in Figure 21, the other polarity must now be checked using the same approach discussed in Section 7.3.1. It should be noted that on many systems, there is a separate factor/offset value for the negative polarity. In this example, it is assumed that there is a separate factor/offset. The negative checks follow a similar flow to the positive checks in that the large verification module is checked first. In this case, all the small verification checks are done afterward (instead of checking the small verification module first at TC 500). Figure 27 shows the initial TC 500 check. Note the change in the trigger edge from rising to falling and the change in the parameters collected to view the fall time (note: use the limits of t_r to check the negative polarity also). From this initial check the I_p is -11.3 amperes (I = -11.6 volts/1.03 ohms). This is a little below target, so the factor is increased to hit closer to the center of the target. This is shown in Figure 28.

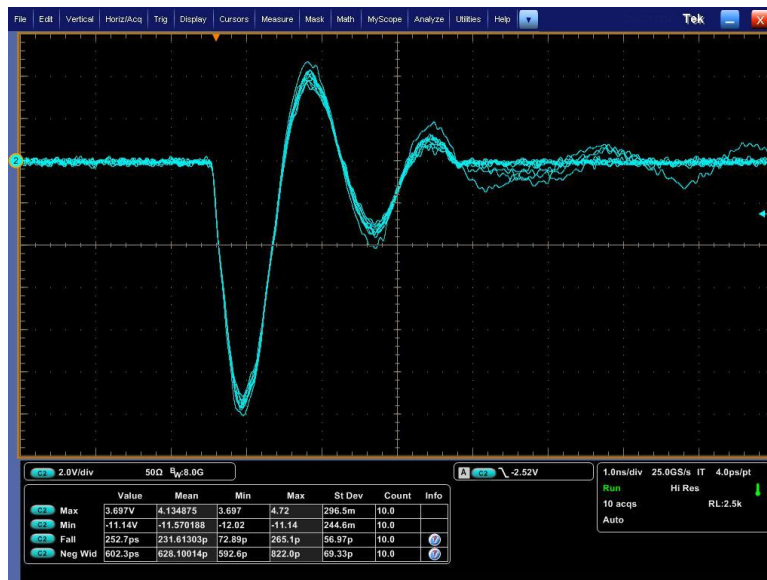


Figure 27: Initial Large Verification Module Reading at Negative TC 500

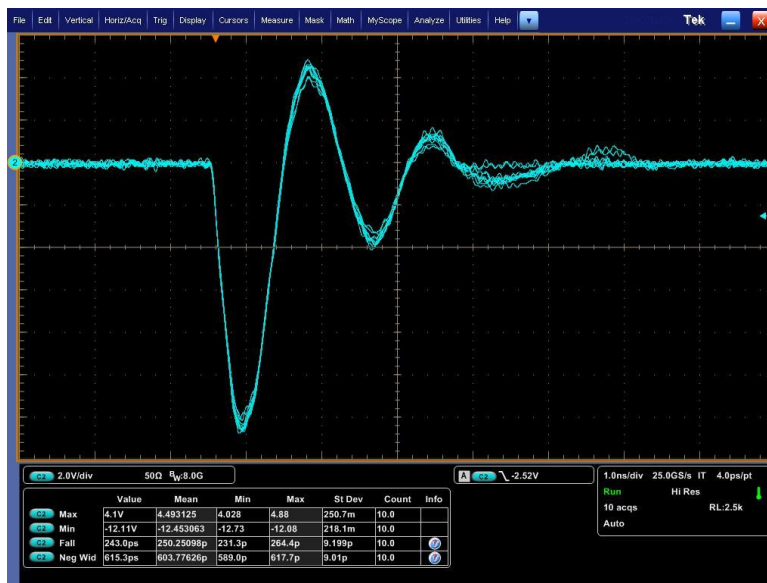


Figure 28: Large Verification Module Reading at Negative TC 500 After Final Factor Adjustment

As can be seen from Figure 28, the I_p is -12.1 amperes ($I = -12.5 \text{ volts}/1.03 \text{ ohms}$). More than close enough to the center of target from Table 1 of JS-002 to run through the other TC conditions for the large verification module. A final factor of 0.83 and offset of 0 volt was used to set the negative TC 500 waveforms shown in Figure 28. As per Figures 15, 17, 19, and 21, which show the verification flows for the TC 125, TC 250, TC 750, and TC 1000 checks, the large verification module is now checked without changing the negative factor/offset (0.83/0 volts). This is followed by the small verification module checks across all five TC conditions. Figures 29, 30, 31, and 32 depict the negative waveform checks for the large verification module at TC 125, TC 250, TC 750, and TC 1000, respectively.

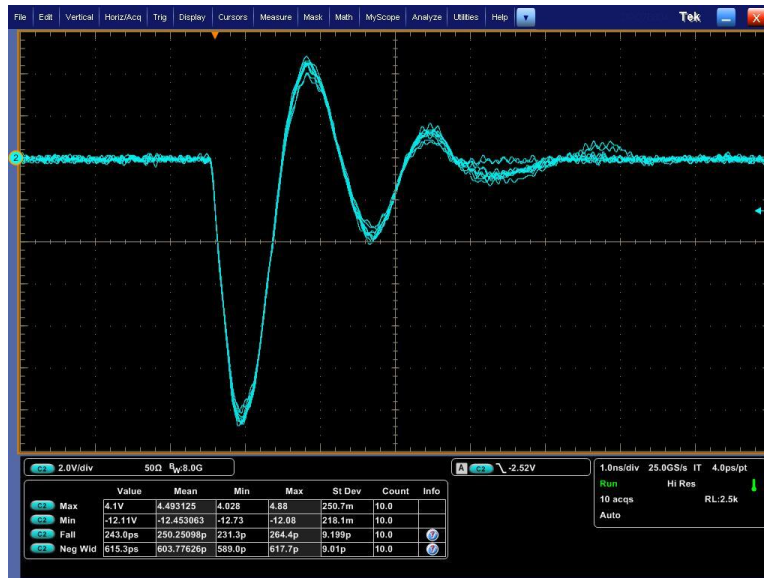


Figure 29: Large Verification Module Reading at Negative TC 125

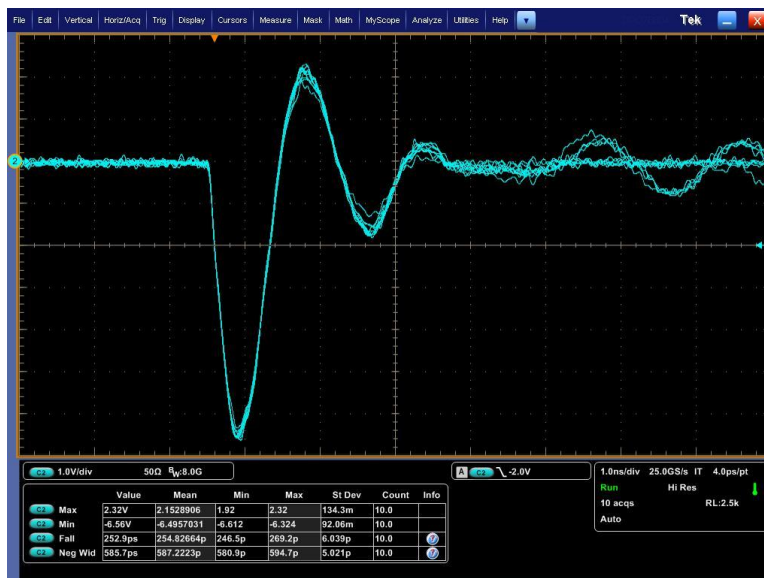


Figure 30: Large Verification Module Reading at Negative TC 250

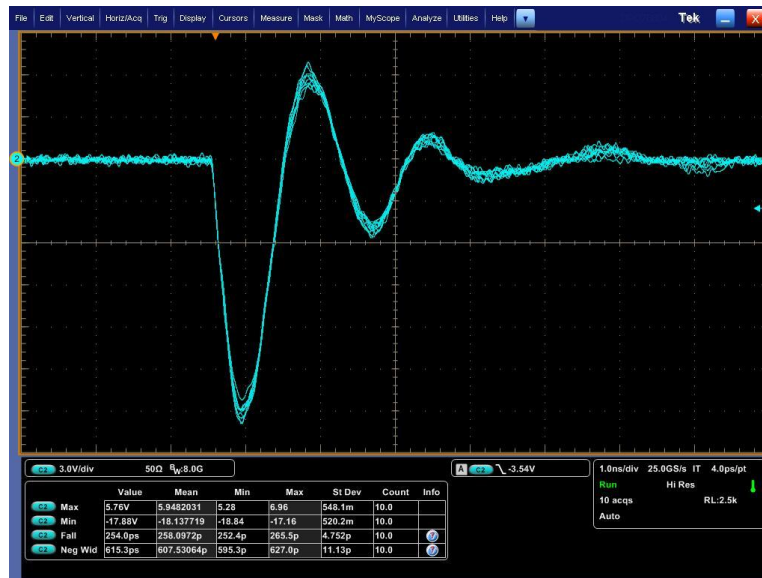


Figure 31: Large Verification Module Reading at Negative TC 750

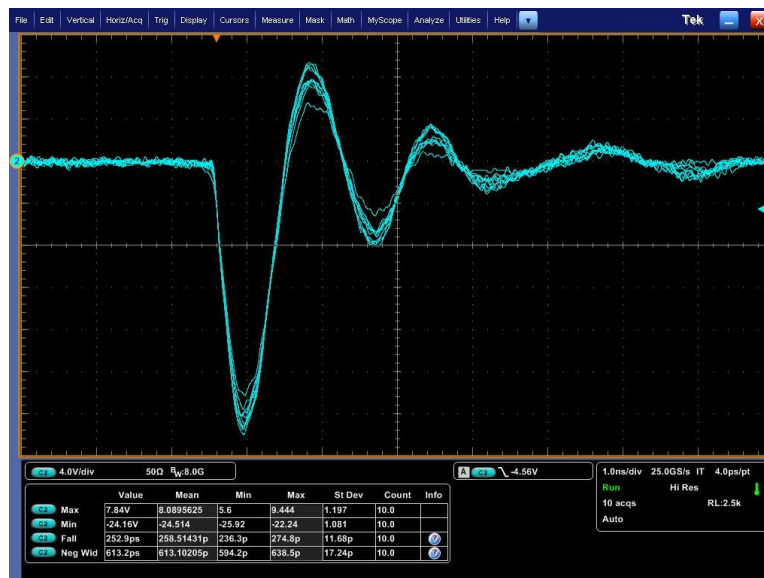


Figure 32: Large Verification Module Reading at Negative TC 1000

Following the final steps in the flow, as shown in Figure 21, the large verification module is completed, and the small verification module is now checked. Figures 33, 34, 35, 36, and 37 depict the negative waveform checks for the small verification module at TC 125, TC 250, TC 500, TC 750, and TC 1000, respectively, using the same factor/offset (0.83/0 volts) as used for the large verification module. Once these checks are completed, all checks have been completed. All results should then be documented for future reference and comparison to later results. This recording is important to understand if factor/offset values change dramatically over time, indicating a bigger problem with the test system.

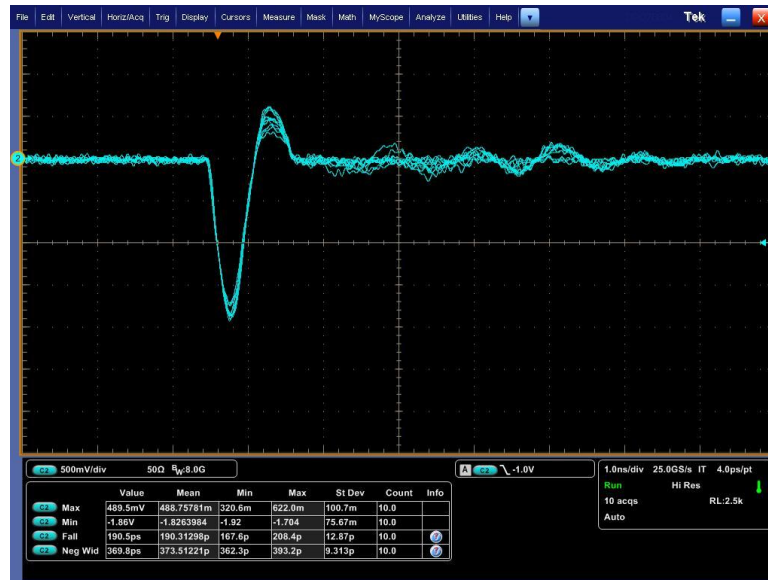


Figure 33: Small Verification Module Reading at Negative TC 125

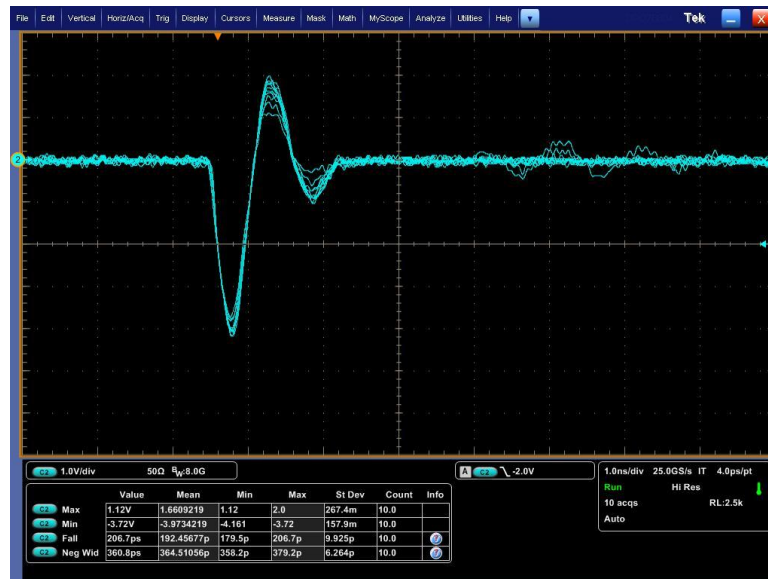


Figure 34: Small Verification Module Reading at Negative TC 250

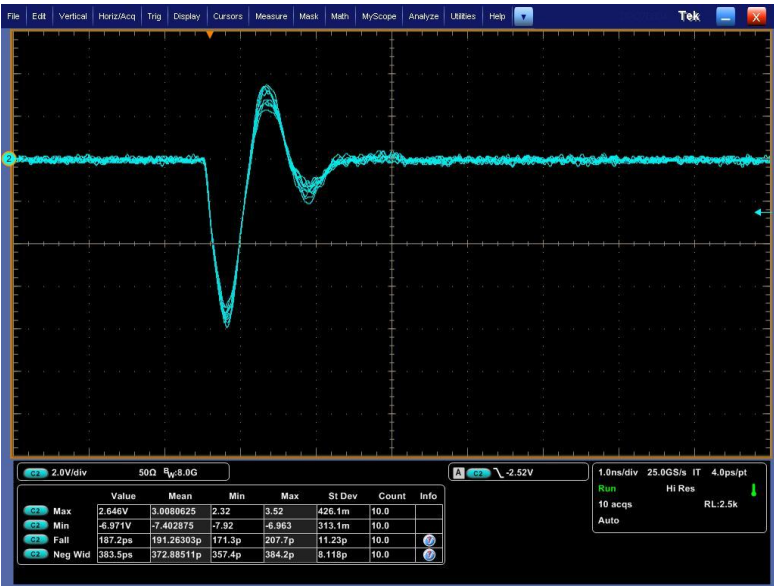


Figure 35: Small Verification Module Reading at Negative TC 500



Figure 36: Small Verification Module Reading at Negative TC 750



Figure 37: Small Verification Module Reading at Negative TC 1000

In reviewing the small verification module, negative waveform results for each are shown in Table 3 (factor = 0.83/offset = 0 volts):

Table 3. Small Verification Module Negative Waveform Summary – Factor/Offset Adjustment Method

Test Condition	I _{peak}	t _r , FWHM and I _{p2}	Figure Reference
TC 125	-1.75 amperes (I = -1.82 volts/1.03 ohms)	Pass	Figure 33
TC 250	-3.9 amperes (I = -4.0 volts/1.03 ohms)	Pass	Figure 34
TC 500	-7.2 amperes (I = -7.4 volts/1.03 ohms)	Pass	Figure 35
TC 750	-10.9 amperes (I = -11.2 volts/1.03 ohms)	Pass	Figure 36
TC 1000	-14.2 amperes (I = -14.6 volts/1.03 ohms)	Pass	Figure 37

In reviewing the large verification module, negative waveform results for each are shown Table 4 (factor = 0.83/offset = 0 volts):

Table 4. Large Verification Module Negative Waveform Summary – Factor/Offset Adjustment Method

Test Condition	I _{peak}	t _r , FWHM and I _{p2}	Figure Reference
TC 125	-3.0 amperes (I = -3.1 volts/1.03 ohms)	Pass	Figure 29
TC 250	-6.3 amperes (I = -6.5 volts/1.03 ohms)	Pass	Figure 30
TC 500	-12.1 amperes (I = -12.5 volts/1.03 ohms)	Pass	Figure 28
TC 750	-17.6 amperes (I = -18.1 volts/1.03 ohms)	Pass	Figure 31
TC 1000	-23.8 amperes (I = -24.5 volts/1.03 ohms)	Pass	Figure 32

It should be noted here that while ANSI/ESDA/JEDEC JS-002 only shows a t_r in Table 1, the implication is that the requirement applies to checking negative waveforms also.

8.0 WAVEFORM VERIFICATION PROCEDURE – SOFTWARE VOLTAGE

8.1 Software Voltage Adjustment Method

This procedure does not adjust the factor/offset. However, it leaves the factor/offset with a value that does not impact the field plate voltage (typically a factor set to 1 and an offset set to 0 volts) and uses the software voltage entry as the primary adjustment of the field plate voltage. This method allows for much more accurate targeting of the I_p range midpoint as defined in Table 1 of ANSI/ESDA/JEDEC JS-002. Still, it creates complexity in determining the correct software voltage entry between the five Test Conditions. Determining software voltage entries other than the five Test Condition levels (discussed in this procedure) requires linear interpolation/extrapolation.

The requirements/details of this software voltage adjustment method are as follows:

- A unique software voltage setting is determined for each Test Condition.
- Unique voltage settings may be used for each polarity (at each TC), but both polarities must be checked.
- The same software voltage setting must be used for both large and small verification modules at each Test Condition.
- Testing at levels other than the five Test Conditions requires a linear interpolation/extrapolation to determine the correct software voltage entry.

The pros/cons of this approach are listed below:

- Pros
 - It can be a more accurate targeting of the mid-range I_p target of each TC.
- Cons
 - Requires interpolation/extrapolation of software voltages needed at Test Conditions other than the five target TCs. So, if experiments are planned in which non-standard voltages are planned, this method can be more cumbersome.

Figure 38 shows the full qualification or quarterly flow check that must be completed in order to follow the requirements called out in ANSI/ESDA/JEDEC JS-002. This section of the user guide steps the user through this flow, step by step, to help better understand what is expected of the

user. Note that while the flow in Figure 38 shows completing the large or small verification module first, then completing the other, any combination of checking the large and small verification module is acceptable as long as all TCs are completed for both verification modules and the requirements listed previously for this adjustment method are met.

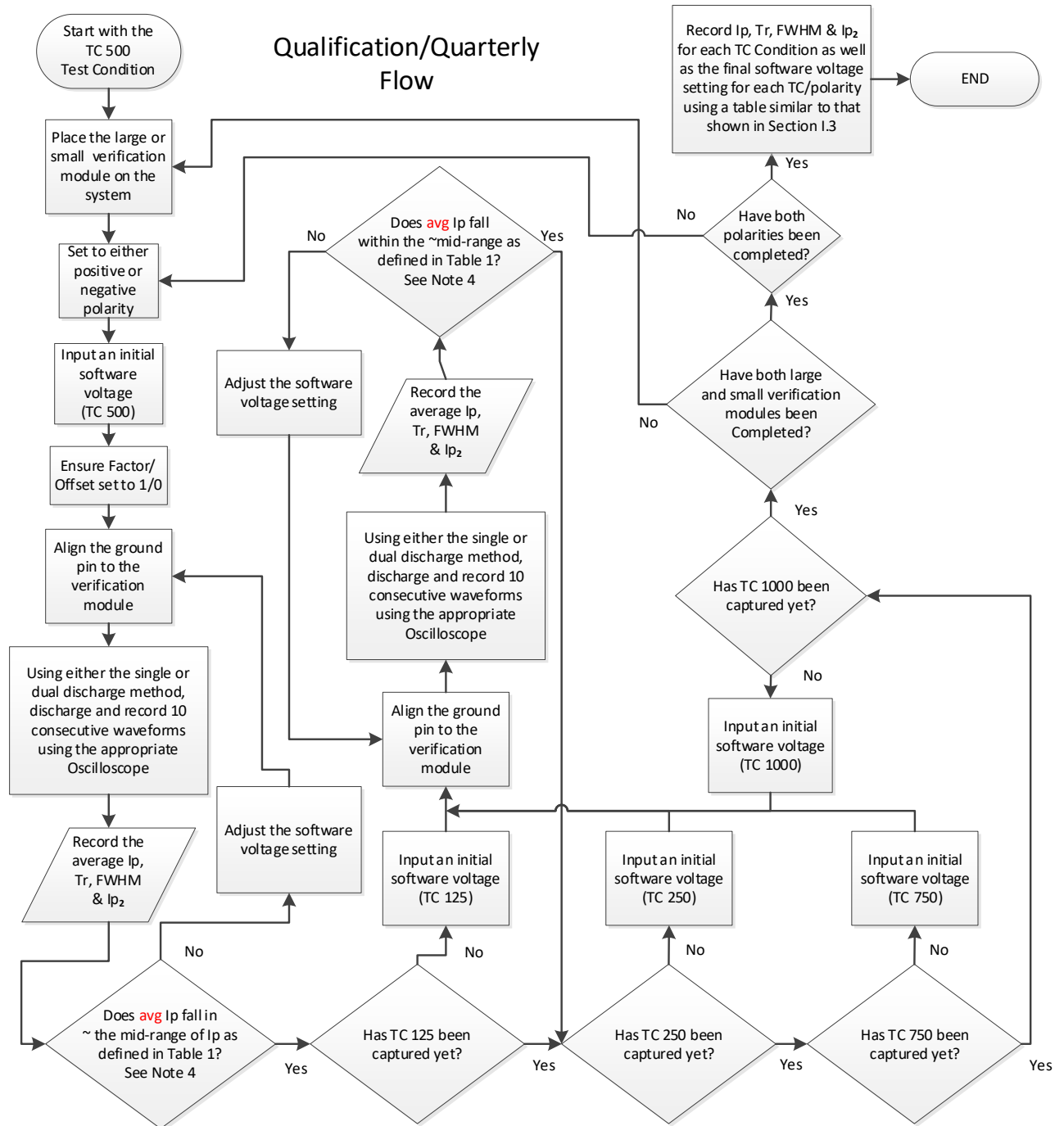


Figure 38: Example Waveform Verification Flow for Qualification and Quarterly Checks Using the Software Voltage Adjustment Method

NOTE 4: After several iterations through this loop, if the user cannot meet the I_p range as defined in Table 1 of ANSI/ESDA/JEDEC JS-002, or that the software voltage setting is well outside the typical documented range, re-clean the verification modules and pogo pin and check that all connections are tight. If this still does not work, check the system vacuum or replace the pogo pin. Consult the tester manufacturer for more information.

8.2 Software Voltage Adjustment Method Details

Figure 39 breaks out the first leg of the flow chart shown in Figure 38, isolating the first check at TC 500. The check can start with any TC as this method sets each TC independently based on determining the optimal software voltage needed to hit the mid-point of Table 1 of ANSI/ESDA/JEDEC JS-002. For this example, the user guide follows the flow shown in Figure 38 and starts with TC 500.

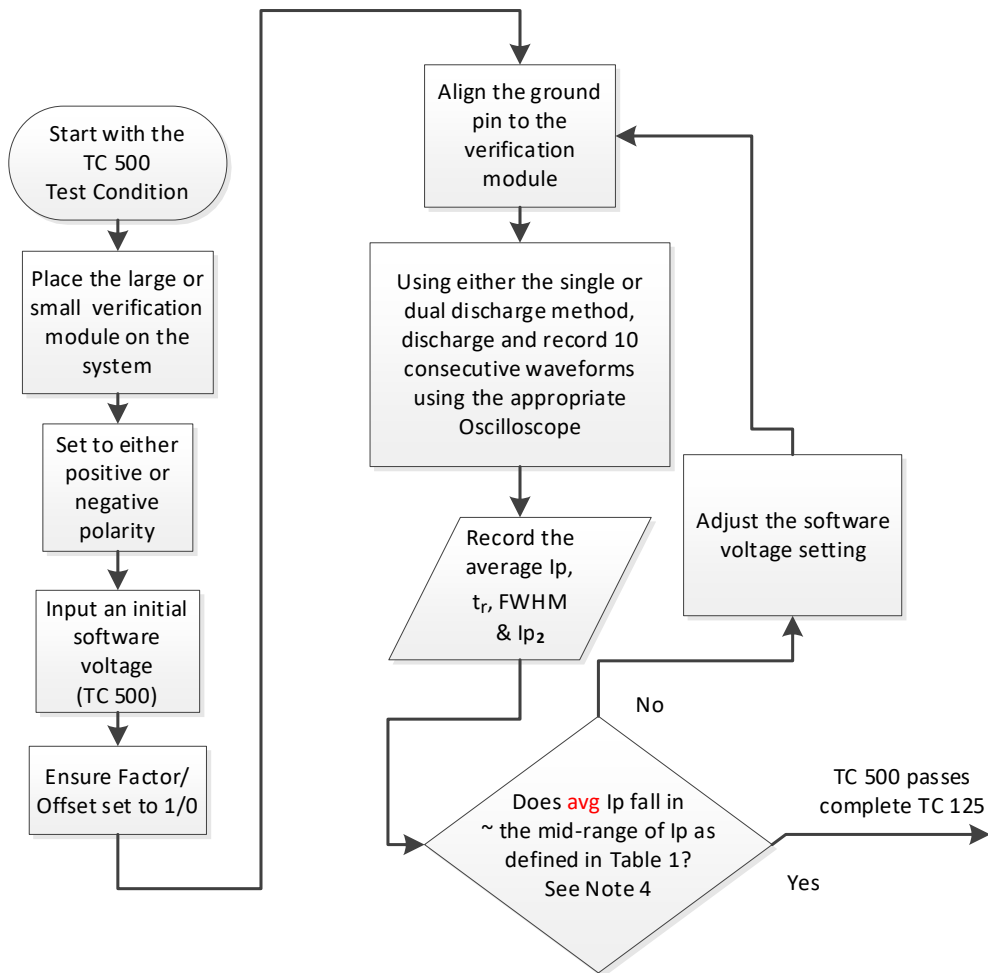


Figure 39: Example TC 500 Verification Flow for Qualification and Quarterly Checks Using the Software Voltage Adjustment Method

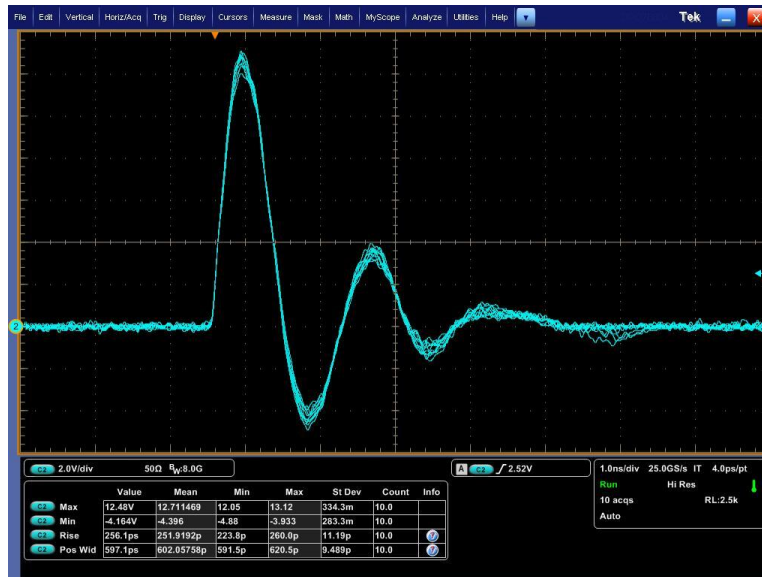
The objective in this first step is to try and adjust the software voltage to align the TC 500 setting to the mid-point of the target range, as shown in Table 1 in ANSI/ESDA/JEDEC JS-002. This is repeated for each TC. It is copied here just for ease of reference from ANSI/ESDA/JEDEC JS-002. Please see the note after Table 1 regarding the interpretation of t_r (rise time) of the waveform.

Table 1 of ANSI/ESDA/JEDEC JS-002 (Copied here for ease of reference)

		Test Condition									
		TC 125		TC 250		TC 500		TC 750		TC 1000	
Verification Module	Sym.	Small	Large	Small	Large	Small	Large	Small	Large	Small	Large
Peak Current (amperes)	I_p	1.4-2.3	2.3-3.8	2.9-4.3	4.8-7.3	6.1-8.3	10.3-13.9	9.2-12.4	15.5-20.9	12.2-16.5	20.6-27.9
Rise time (ps)	t_r	<250	<350	<250	<350	<250	<350	<250	<350	<250	<350
Full width at half maximum (ps)	FWHM	250-600	450-900	250-600	450-900	250-600	450-900	250-600	450-900	250-600	450-900
Undershoot (A, max. 2nd peak)	I_{p2}	<70 % I_p	<50% I_p	<70 % I_p	<50% I_p	<70 % I_p	<50% I_p	<70 % I_p	<50% I_p	<70 % I_p	<50% I_p

NOTE: t_r also refers to the similar first peak transition time to a negative maximum for the negative going CDM first peak pulse.

Figure 40 shows an example of the first set of 10 waveforms captured when collecting the TC 500 condition on the large verification module. Figure 40 shows the raw voltage measurements and must be adjusted for the correct resistance in the discharge head ($I = V/R$). For all the examples shown in this section, the resistance of the discharge head is 1.03 ohms.

**Figure 40: Initial Large Verification Module at TC 500**

NOTE: Software Voltage = 420 Volts

As can be seen, the initial I_p is a little on the high side, running at an average value of 12.3 amperes ($I = 12.7 \text{ volts}/1.03 \text{ ohms}$) for the average of the ten waveforms compared to a target of 12.1 amperes. This was using a software voltage of 420 volts. It should be noted here that not all ten waveforms must be within specifications, but the average must be. The reading is not expected to be 12.1 amperes. However, the value of 12.3 amperes is a little on the high side since the objective here is to try and hit the mid-point of the Table 1 target range of ANSI/ESDA/JEDEC JS-002.

Figure 41 shows the result after a decrease in the software voltage to 410 volts. In this case, the average I_p is now 12.0 amperes ($I = 12.4 \text{ volts}/1.03 \text{ ohms}$).

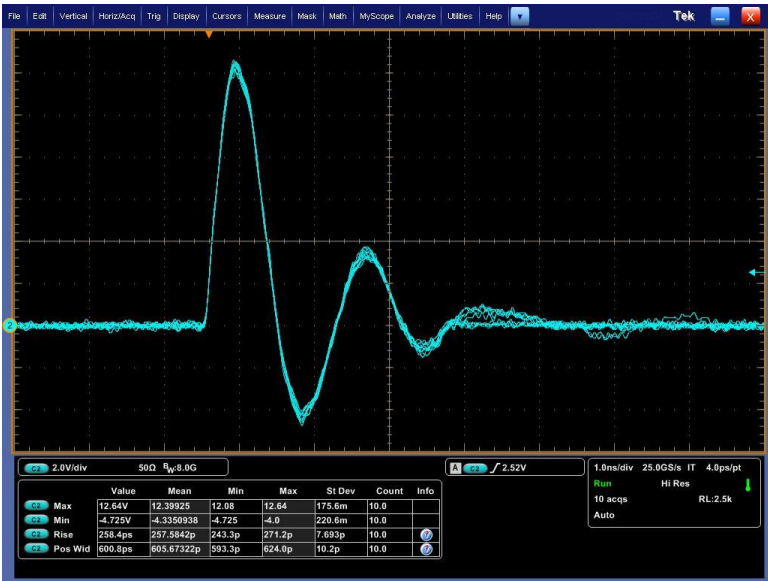


Figure 41: Large Verification Module at TC 500 After Initial Software Voltage Adjustment to 410 Volts

With one more adjustment in the software voltage to 415 volts, a final I_p of 12.2 amperes is achieved ($I = 12.6 \text{ volts}/1.03 \text{ ohms}$). This is accurate enough to start checking other TC conditions. This is shown in Figure 42.

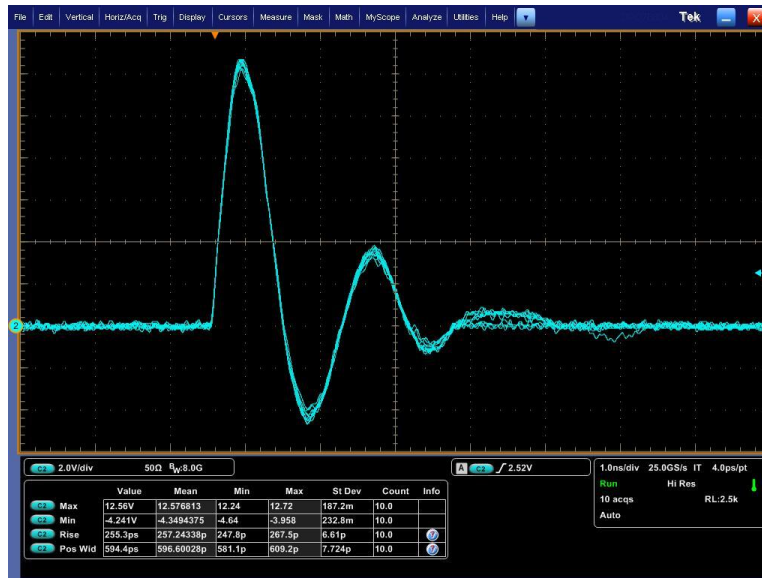


Figure 42: Large Verification Module at TC 500 After Final Software Voltage Adjustment of 415 Volts

According to Figure 38, the next step in the flow would be to check the large verification module at all other TC conditions, starting with TC 125 (see Figure 38). However, since the same software voltage must be used for both the small and large verification modules, it is prudent to check the small verification module. This is done now to verify that 415 volts for a software voltage is a reasonable value.

Figure 43 shows a check of the small verification module at TC 500 before moving on to the TC 125 check. The I_p shown is 7.4 amperes ($I = 7.6 \text{ volts}/1.03 \text{ ohms}$). Well within the target range and very near the mid-point. With this reading, it was concluded that moving on to the TC 125 check makes sense.

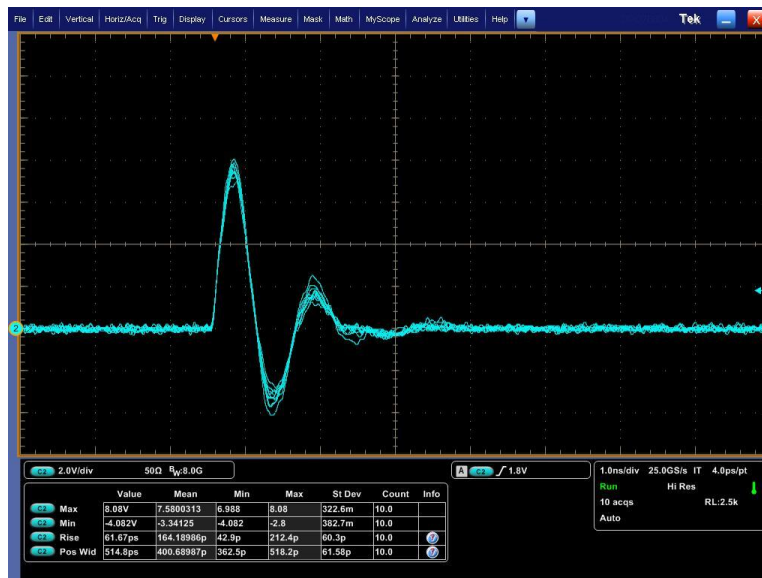


Figure 43: Small Verification Module at TC 500 After Final Software Voltage Adjustment of 415 Volts

Once the TC 500 is completed, the user can move on to TC 125, as shown in Figure 44. The procedure in Figure 38 suggests checking the small verification module after all the large verification module checks are completed (or the large verification module after all small verification module checks). This procedure checks both verification modules after each TC.

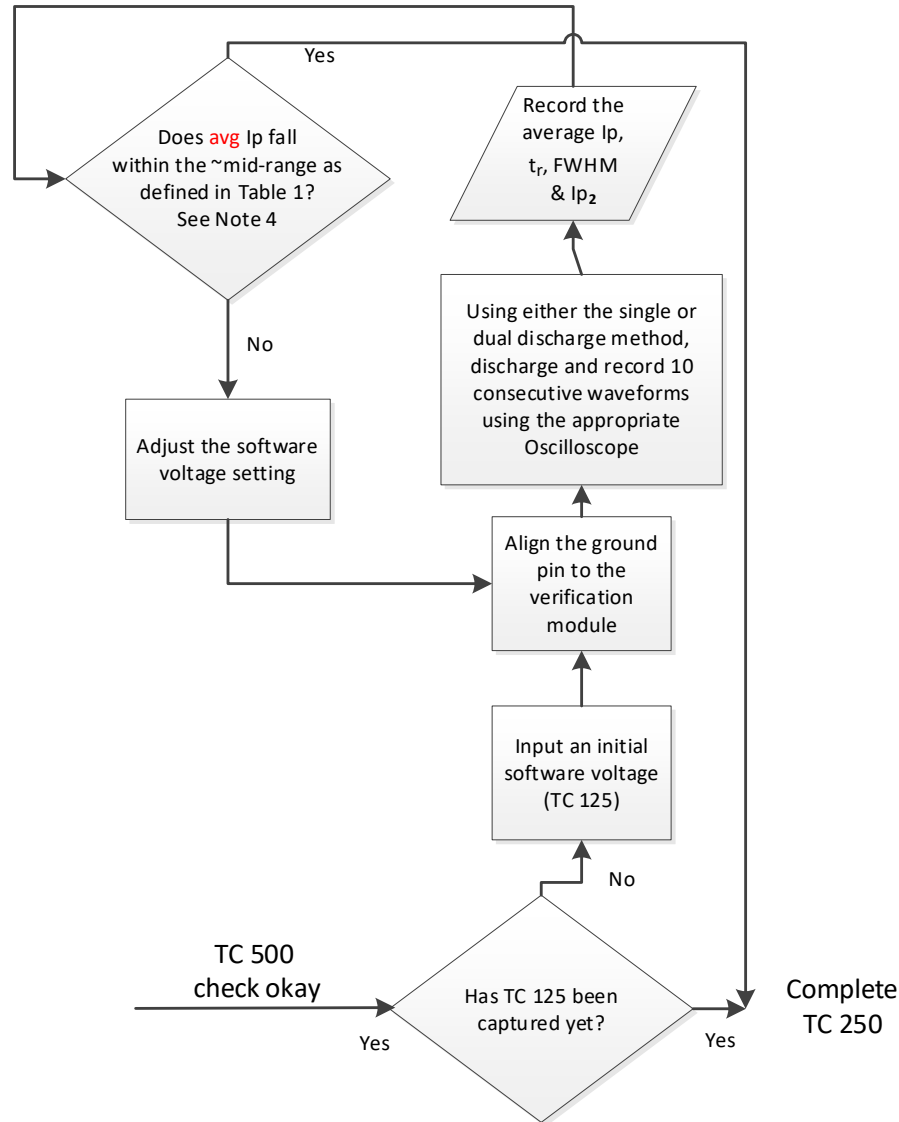


Figure 44: Example TC 125 Verification Flow for Qualification and Quarterly Checks Using the Software Voltage Adjustment Method

Following the procedure in Figure 44, the TC 125 is completed next, after a few iterations with the software voltage setting. A value of 105 volts was determined to be the best value. The large verification module waveforms are shown in Figure 45. The small verification module waveforms are shown in Figure 46. The I_p for Figure 45 is 3.0 amperes ($I = 3.1$ volts/1.03 ohms) and the I_p for Figure 46 is 1.90 amperes ($I = 1.95$ volts/1.03 ohms), right on target for the mid-point of TC 125.

This same flow shown in Figure 44 can then be used to complete the software settings for TC 250, TC 750, and TC 1000. These results are shown in Figures 47 to 52.

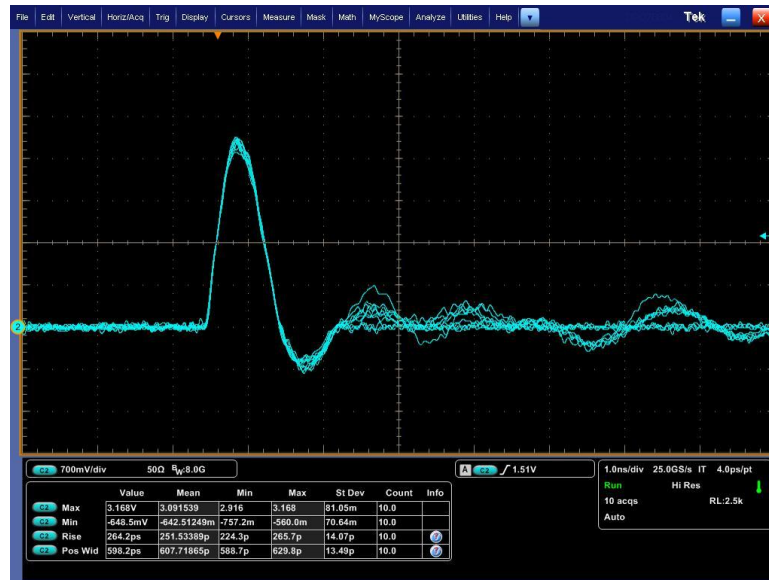


Figure 45: Large Verification Module at TC 125 After Final Software Voltage Adjustment of 105 Volts

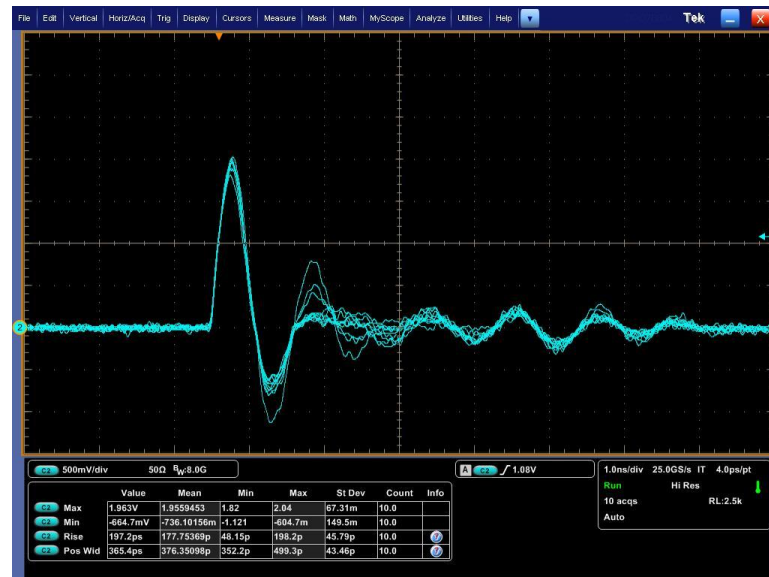


Figure 46: Small Verification Module at TC 125 After Final Software Voltage Adjustment of 105 Volts

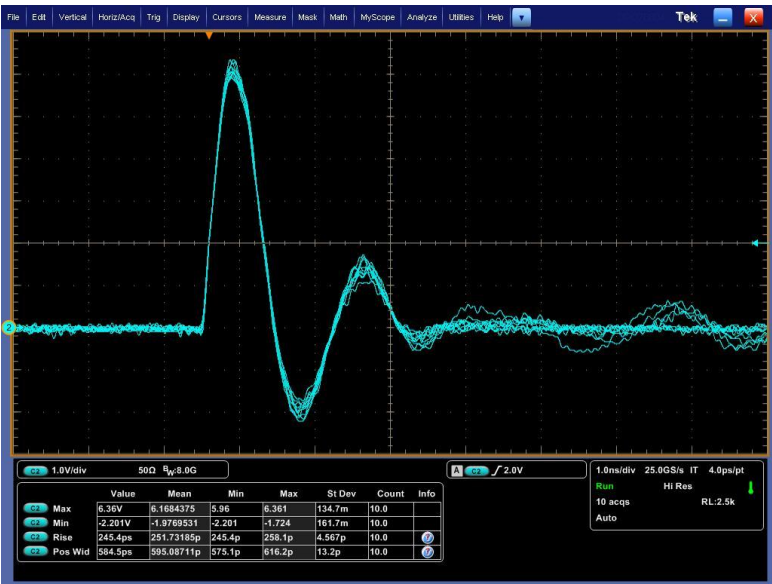


Figure 47: Large Verification Module at TC 250 After Final Software Voltage Adjustment of 200 Volts

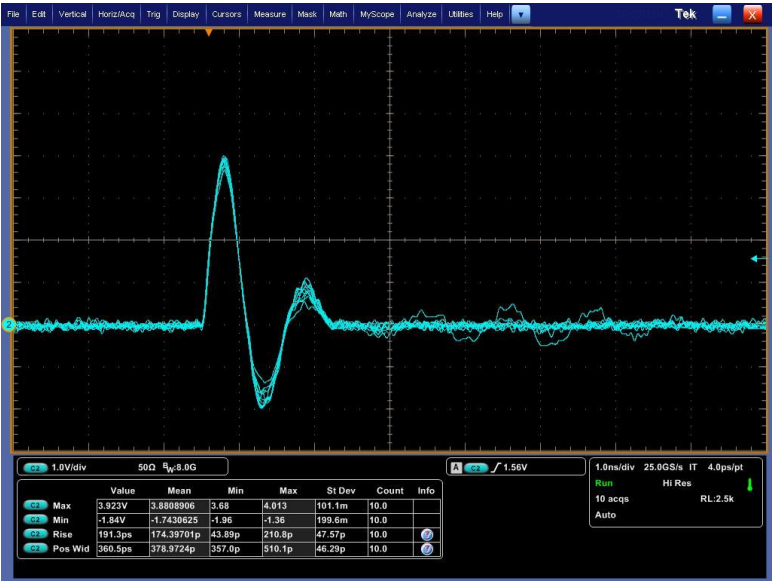


Figure 48: Small Verification Module at TC 250 After Final Software Voltage Adjustment of 200 Volts

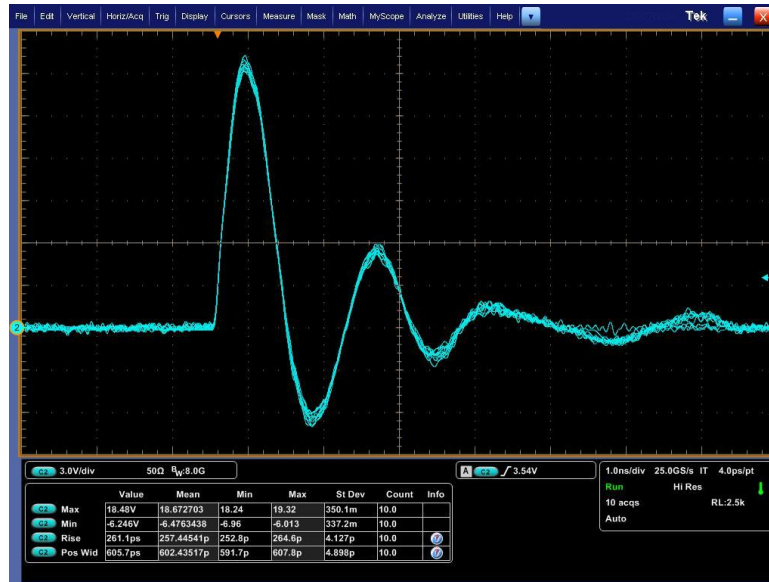


Figure 49: Large Verification Module at TC 750 After Final Software Voltage Adjustment of 615 Volts

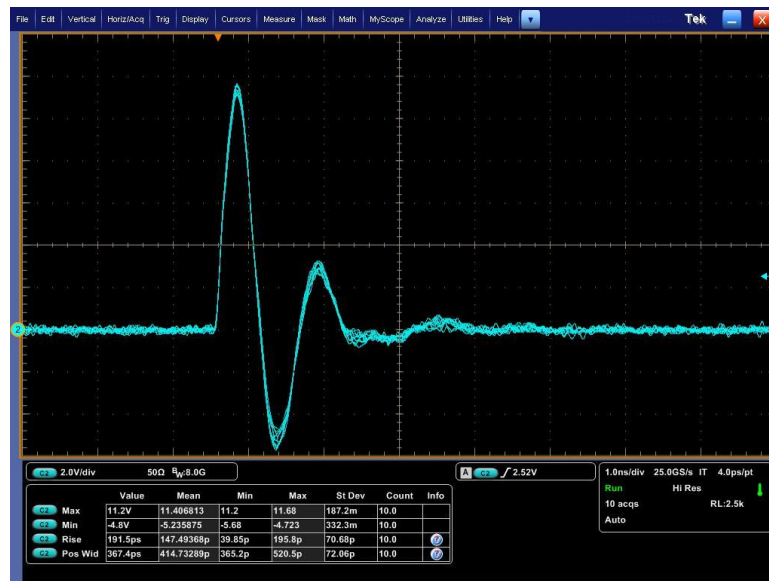


Figure 50: Small Verification Module at TC 750 After Final Software Voltage Adjustment of 615 Volts

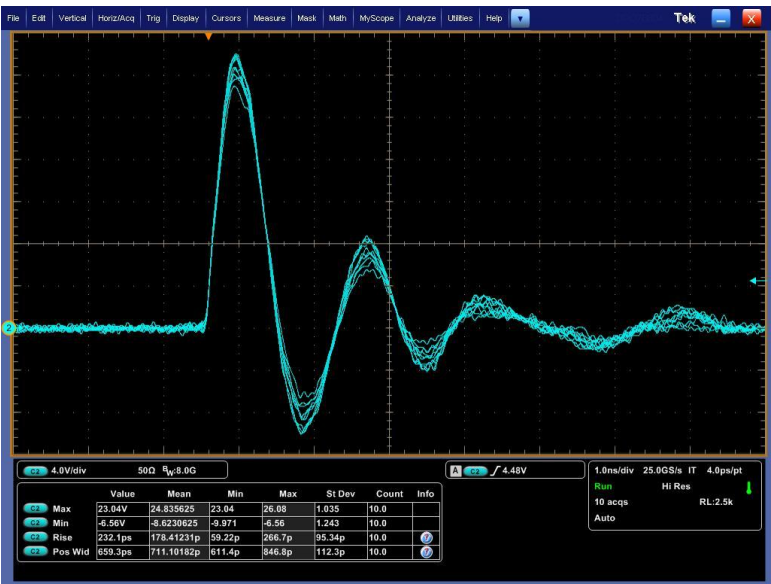


Figure 51: Large Verification Module at TC 1000 After Final Software Voltage Adjustment of 815 Volts

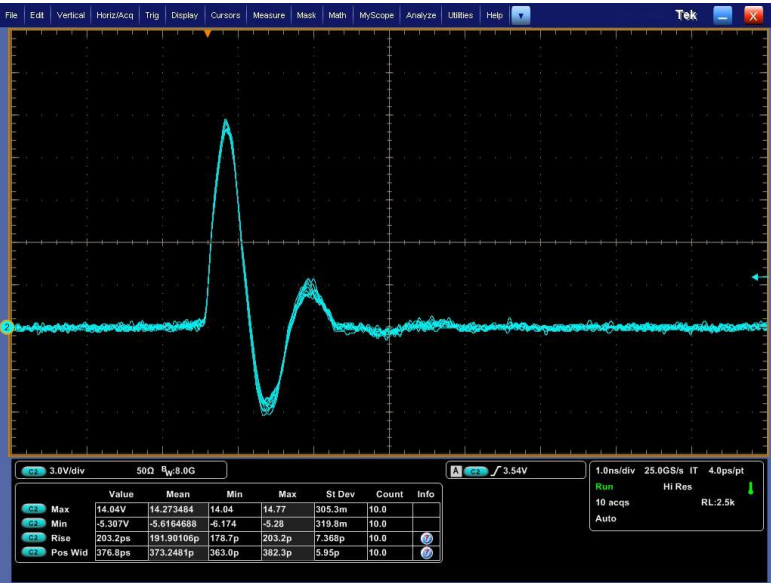


Figure 52: Small Verification Module at TC 1000 After Final Software Voltage Adjustment of 815 Volts

Figures 47 and 48 depict the large and small verification modules for TC 250. The software voltage needed was 200 volts and resulted in an I_p value of 6.0 amperes ($I = 6.2 \text{ volts}/1.03 \text{ ohms}$) for the large verification module and an I_p value of 3.8 amperes ($I = 3.9 \text{ volts}/1.03 \text{ ohms}$) for the small verification module. Figures 49 and 50 depict the large and small verification modules for TC 750. The software voltage needed was 615 volts and resulted in an I_p value of 18.1 amperes ($I = 18.7 \text{ volts}/1.03 \text{ ohms}$) for the large verification module and an I_p value of 11.1 amperes ($I = 11.4 \text{ volts}/1.03 \text{ ohms}$) for the small verification module. Figures 51 and 52 depict the large and small verification modules for TC 1000. The software voltage needed was 815 volts and resulted in an I_p value of 24.1 amperes ($I = 24.8 \text{ volts}/1.03 \text{ ohms}$) for the large verification module and an I_p value of 13.9 amperes ($I = 14.3 \text{ volts}/1.03 \text{ ohms}$) for the small verification module. All values are

very close or right on the mid-point of the Table 1 values of ANSI/ESDA/JEDEC JS-002, and these values would be very reasonable to start testing the product through CDM testing. Below is a summary of all the results for the software voltage adjustment method for a positive waveform verification.

Software voltage values:

- For TC 125: 105 volts
- For TC 250: 200 volts
- For TC 500: 415 volts
- For TC 750: 615 volts
- For TC 1000: 815 volts

For the small verification module, positive waveform results for each TC are shown in Table 5.

Table 5. Small Verification Module Positive Waveform Summary – Software Voltage Adjustment Method

Test Condition	I _{peak}	t _r , FWHM and I _{p2}	Figure Reference
TC 125	1.90 amperes (I = 1.95 volts/1.03 ohms)	Pass	Figure 46
TC 250	3.8 amperes (I = 3.9 volts/1.03 ohms)	Pass	Figure 48
TC 500	7.4 amperes (I = 7.6 volts/1.03 ohms)	Pass	Figure 43
TC 750	11.1 amperes (I = 11.4 volts/1.03 ohms)	Pass	Figure 50
TC 1000	13.9 amperes (I = 14.3 volts/1.03 ohms)	Pass	Figure 52

For the large verification module, positive waveform results for each TC are shown in Table 6.

Table 6. Large Verification Module Positive Waveform Summary – Software Voltage Adjustment Method

Test Condition	I _{peak}	t _r , FWHM and I _{p2}	Figure Reference
TC 125	3.0 amperes (I = 3.1 volts/1.03 ohms)	Pass	Figure 45
TC 250	6.0 amperes (I = 6.2 volts/1.03 ohms)	Pass	Figure 47
TC 500	12.2 amperes (I = 12.6 volts/1.03 ohms)	Pass	Figure 42
TC 750	18.1 amperes (I = 18.7 volts/1.03 ohms)	Pass	Figure 49
TC 1000	24.1 amperes (I = 24.8 volts/1.03 ohms)	Pass	Figure 51

As with the factor/offset adjustment method, the negative waveform parameters must also be completed, and a unique software voltage value can be used for the negative side. However, the

large and small verification modules must both use the same negative software voltage value also. Since this process is the same as what was shown for the positive waveform, it is not repeated.

It should be noted here that while ANSI/ESDA/JEDEC JS-002 only shows t_r in Table 1, the implication is that the requirement applies to checking negative waveforms also.

8.3 Estimation of Test Voltages Other Than the ANSI/ESDA/JEDEC JS-002 Test Conditions

As can be seen, the mid-point target value is met more closely by using a unique software voltage setting for each TC. The challenge comes when CDM voltage levels other than the TCs are desired to be tested. The user must now interpolate/extrapolate the correct software voltage setting for each unit's test voltage needed. This requires the user to create a plot of target voltage versus software voltage, as shown in Figure 53, and generate the simple line equation to calculate the correct software voltage for any given target test voltage. The values derived from the above example were used to create Figure 53. The extracted equation, $y = 0.8159x + 1.6768$, can then be used to calculate any given software voltage setting for the desired target test voltage. It should be noted that it is unnecessary to create a plot of all five TC conditions to generate this equation. A well-centered set of data would produce nearly the same equation with just two data points. Thus, the estimation of the target software voltage between two TCs can be derived using an equation with the data from the TC on either side of the desired "in-between" target level. While this approach is relatively straightforward, the risk comes in ensuring the right equation is used for positive and negative. Also, it is important to understand that the equation may change with each quarterly verification as well as on each CDM tester in the lab – resulting in more chance for human error.

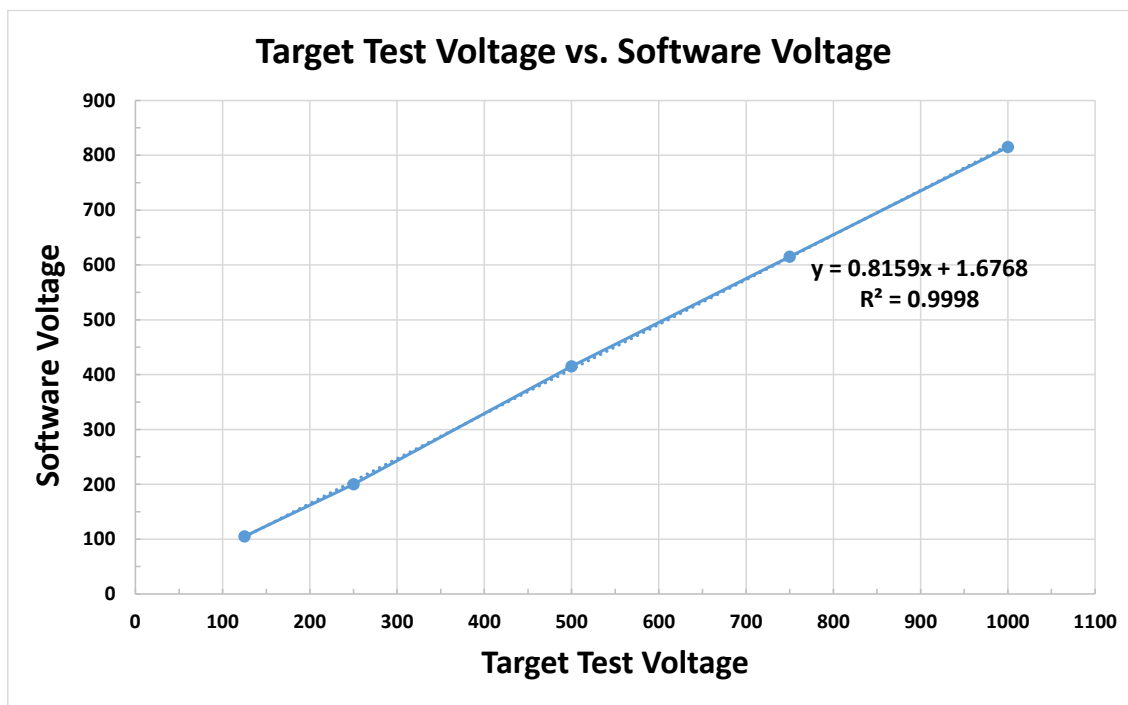


Figure 53: Example Plot of Software Voltage Versus Target Test Voltage Used for the Software Voltage Adjustment Method

9.0 PACKAGE VARIABLES AFFECTING FICDM PEAK CURRENT AND PULSE SHAPE

9.1 Three-Capacitor Model

The CDM test setup creates several capacitors. These capacitors determine the CDM waveform properties in conjunction with spark resistance and inductance of the arc, pogo pin, and package. While several papers have described CDM models with up to five capacitors [4], a basic understanding of the waveform and almost all waveform properties of interest can be explained with the three-capacitor model [5] shown in Figure 54. The three capacitors are:

1. The field plate to DUT capacitor, C_{DUT} , with the FR4 insulator as the dielectric.
2. The discharge head ground plane to DUT capacitor, C_G , with air as the dielectric.
3. The discharge head ground plane to field plate capacitor, C_{FG} , with air as the dielectric.

As DUT size increases, all three capacitors in the three-capacitor model change. As DUT size increases, C_{DUT} increases, although the value of C_{DUT} depends on many factors, as discussed below. As the DUT size increases, C_G also increases but is always less than C_{DUT} . C_{FG} decreases with increasing DUT size as the DUT blocks electric field lines between the field plate and the ground plane.

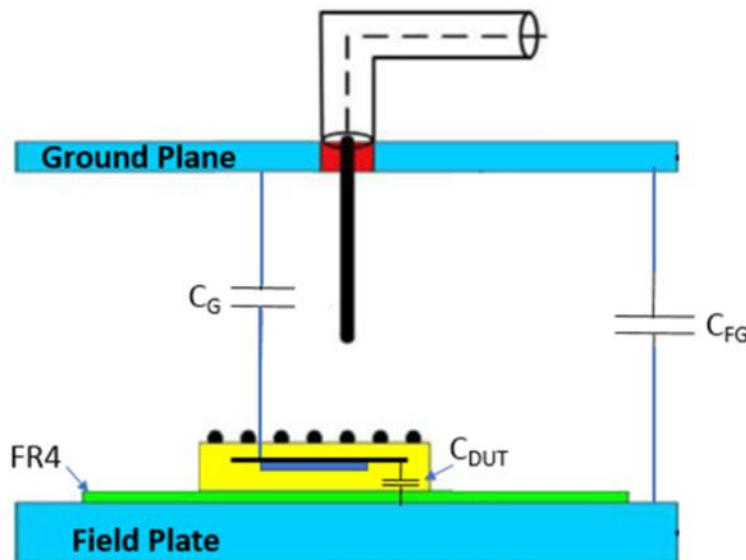


Figure 54: Illustration of the FICDM Capacitors

The relative sizes of the three capacitors determine the nature of the CDM discharge. Before discussing how the relative sizes of the three capacitors affect waveform properties, it is necessary to understand the sequence of events during a CDM test, especially during the pulse itself.

1. Uncharged DUT is placed on an insulator on the field plate, which is at 0 volts. Steps 2 through 11 then describe the events that take place by the FICDM test system.
2. The potential of the field plate is brought to a high potential by a high voltage power supply through a high-value resistor.
 - a. C_{FG} is charged to the test voltage.
 - b. Series capacitors C_G and C_{DUT} are charged to the test voltage.
3. Since C_{DUT} is much larger than C_G , most of the voltage drop between the field plate and the ground plane is across C_G .
 - a. The voltage on the DUT is, therefore, close to the field plate voltage.
 - b. The total charge on the DUT is still zero.

4. From this step until step 10, the Field Plate can be considered disconnected from the power supply due to the high-value resistor and the fast nature of the CDM event.
5. The pogo pin is lowered until an arc forms between the pogo pin and the DUT pin.
6. Current flows until the DUT is at ground potential.
7. If the DUT voltage is zero:
 - a. The voltage across C_G is zero.
 - b. The voltage across the series combination of C_{DUT} and C_{FG} is zero.
8. The grounding of the DUT means that the voltage across C_{DUT} has increased.
9. The charge to increase the voltage across C_{DUT} comes from three places.
 - a. The pogo pin is on the top side of C_{DUT} (this is the measured CDM current).
 - b. C_G on the top side of C_{DUT} (only important for very large DUTs).
 - c. C_{FG} on the bottom side of C_{DUT} (due to the high resistance between the power supply and the field plate, the power supply supplies no current during the CDM event's time scale).
10. As C_{FG} supplies charge to C_{DUT} , the field plate voltage drops until the total voltage across C_G and C_{DUT} is zero.
11. Over microseconds to milliseconds, the power supply returns the field plate voltage to the CDM test voltage.

It is possible to understand how the CDM pulse varies with the DUT size knowing the above sequence.

For a very small DUT, C_{DUT} is considerably less than C_{FG} . With C_{FG} much larger than C_{DUT} , the charge needed to increase the voltage across C_{DUT} during the CDM event will not significantly change the voltage across C_{FG} . Therefore, for very small C_{DUT} , the amount of charge in the CDM pulse increases roughly linearly with C_{DUT} . Therefore, peak currents are expected to increase approximately linearly, as shown for the small package area in Figure 55 [6,7].

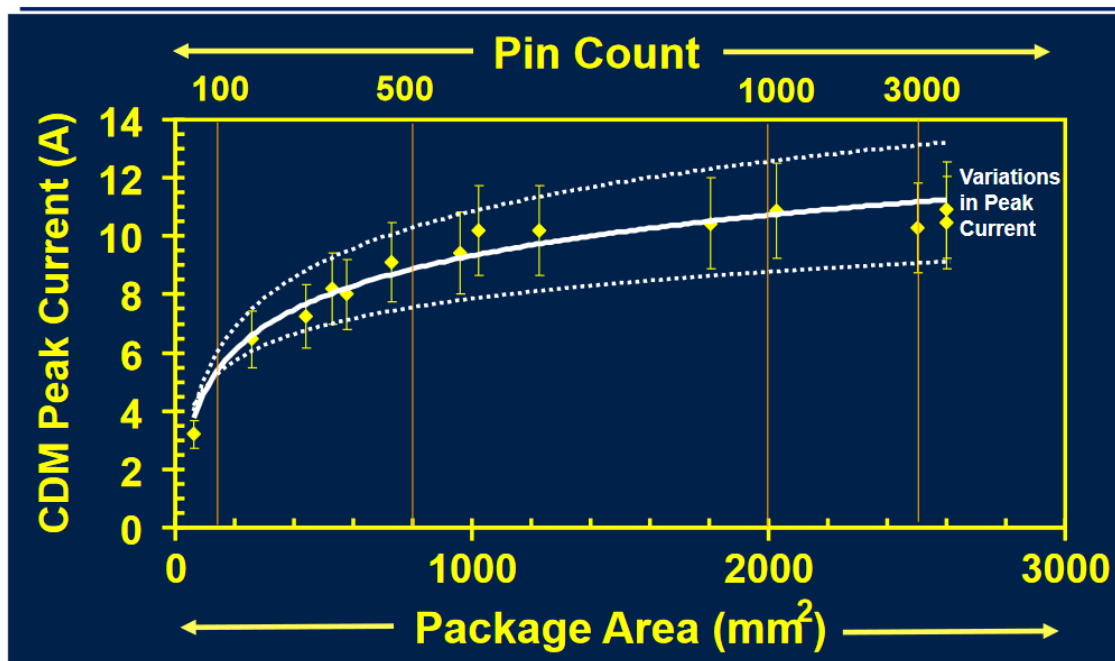


Figure 55: CDM Peak Current for Package Sizes Up to 2600 mm² for 500-Volt Stress

For small to medium size DUTs, C_{DUT} becomes similar to and larger than C_{FG} . When the pulse occurs and the DUT is grounded, C_{FG} needs to supply a large fraction of its charge to C_{DUT} to maintain a net-zero voltage sum across C_{DUT} and C_{FG} . The large reduction in charge on C_{FG} results in the voltage on the Field Plate dropping significantly during the pulse, and the charge in the CDM pulse saturates as C_{DUT} increases. This accounts for some of the saturation in the peak current as the device area increases. This is shown in Figure 55.

The peak current is not, however, purely determined by the capacitance values. Inductance is also a critical factor in understanding CDM pulse shapes. Except for very large DUTs, C_{FG} is usually much larger than C_G . In these cases, the main current path is a loop from the ground plane, through the pogo pin, C_{DUT} , C_{FG} , and back to the Ground Plane. This path is a classic LCR circuit. The 1-ohm sense resistor and the arc provide resistance, the pogo pin and the arc provide inductance, and the series combination of C_{DUT} and C_{FG} provides the capacitor. Most CDM pulses are a damped, but not overdamped, oscillation. The frequency of the oscillation is proportional to $1/\sqrt{LC}$. Assuming the L to be insensitive to DUT size, we can expect the oscillation frequency to decrease as C_{DUT} increases. This is exactly what is observed. As C_{DUT} increases, the first peak of the CDM pulse gets wider. In fact, at the smallest size devices, pulse widths are a small fraction of a nanosecond and is a major reason ANSI/ESDA/JEDEC JS-002 requires a 6-GHz or higher oscilloscope. The combination of the increased value of C_{DUT} with larger size and the inductance of the pogo pin and arc account for the saturation in peak current shown in Figure 55.

9.2 Internal Package Impedance and Die Circuit Effects

The details of an individual integrated circuit can affect CDM pulse properties. Different types of integrated circuit packages can have very different capacitance for the same area of the package body. Figure 56 shows the peak current versus the surface area touching the field plate for 74 different packages at 500 volts. The data is equally split between leaded and leadless packages. The data was collected at a single test lab within a large semiconductor manufacturer.

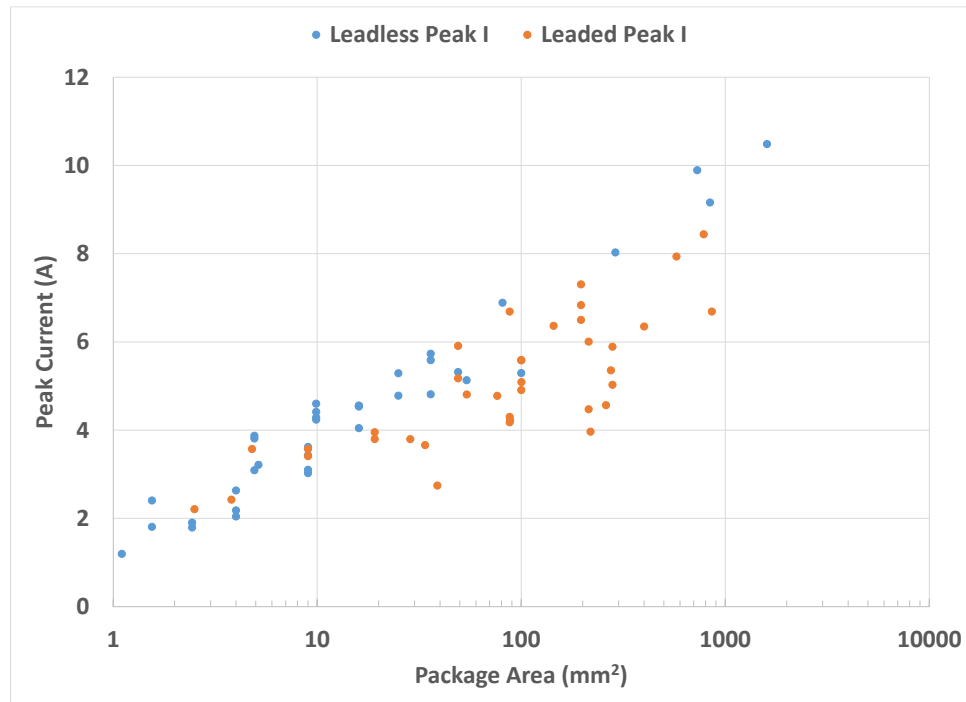


Figure 56: Effect of Leaded/Leadless Packages on Peak Current Versus Package Area at 500 Volts

All peak currents for the leadless packages fall within a relatively narrow band over three orders of magnitude of package area. The peak currents for the leaded packages show considerably more scatter. The largest peak currents for the leaded packages appear to be bounded by the same maximum peak current as the leadless packages. The scatter in the leaded package data is consistently toward lower peak currents. This data implies several things.

Package trends over the last two decades have been moving consistently toward the leadless package. The newer, leadless packages also tend to be thinner. This results in a higher and more consistent device to field plate capacitance for the same package area.

The peak currents for the leaded packages are always similar to or lower than the peak currents of leadless packages. This indicates that the extra capacitance from the leads extending beyond the package body contributes little to the peak current.

The wide scatter in the peak current for the leaded packages may be the result of three factors. Leaded and often older package types are often thicker, and there is likely a much wider range of thickness between the top of the body of the package and the die and lead frame. This results in a wider range of capacitance for leaded packages of the same area. Leaded packages may also have more inductance, which could result in wider pulses with lower peak current. Additionally, variations in the ratio of leadframe area to mold compound area can also contribute.

A full understanding of the data in Figure 56 would likely require measurement or 3D calculation of the device to field plate capacitance and circuit or 3D simulation of the CDM event, including inductance effects, for a wide variety of package types.

- Peak current is also affected by the impedance of the package routing and die circuit impedances, spark impedance, and any active effects from ESD protection circuit elements such as diodes or clamps. As a consequence, pin type and position affect the peak current response as described below.
- When considering the types of pins in a processor, the VSS pins typically have the lowest impedance to the major sources of field induction in the package. VSS is also often connected to an internal plane or grid, both in the package and the die, which has a low impedance. Consequently, VSS typically have the highest peak current and fastest rise time [6].
- Package/die planes or grids are also often used for VDD. And they typically will couple internally to a VSS plane. As a result, VDD pins can have peak currents and rise times comparable to VSS pins, although this may depend on the power domain area and reactance of the domain to VSS.
- I/O pins often have a lower peak current and greater full width at half maximum (FWHM) due to package routing impedance and the ESD protection circuitry response. Also, pins on the edge or corners of the package often have slightly lower peak currents and greater FWHM than identical pins in the center of the package, with pins on the edge of larger packages being more affected than smaller packages. For I/O pins, transmission line propagation delay and reflections have been cited as potentially lowering peak current, slowing rise time, and increasing FWHM measured on the edge or corner of the package. However, waveforms resulting from these reflections may not accurately depict the current that the I/O protection circuitry experiences during a CDM discharge [8].
- When testing terminals (pads, pins, balls, etc.) on the top side of a device, C_{DUT} , C_G , and C_{FG} may be altered. As a result, the charge time (delay) required to reach saturation, as described in Section 6.0, may be altered compared to the bottom side. When testing terminals on the top side of a device, an evaluation of the charge time (delay) is recommended (as if a new device is being tested for the first time) to ensure that saturation is achieved.

10.0 CALCULATION OF CHARGE AND EFFECTIVE CAPACITANCE

Section 9.0 has already discussed the impacts of C_{DUT} on the overall I_{peak} . Another capacitance derived from the simplified electrical schematic shown in Figure 54 is the effective capacitance (C_{eff}). This can be written as:

$$C_{eff} = \frac{(C_{DUT} * C_{FG})}{(C_{DUT} + C_{FG})} \text{ for cases where } C_{DUT} \gg C_G \quad (1)$$

The total current during a CDM discharge is proportional to the maximum charge that the device can hold, and the charge can be written as:

$$Q = C_{eff} * V \quad (2)$$

Where V is the actual field plate voltage. Calculating charge can be completed from a typical CDM waveform, as shown in Figure 57, by integrating in the following way.

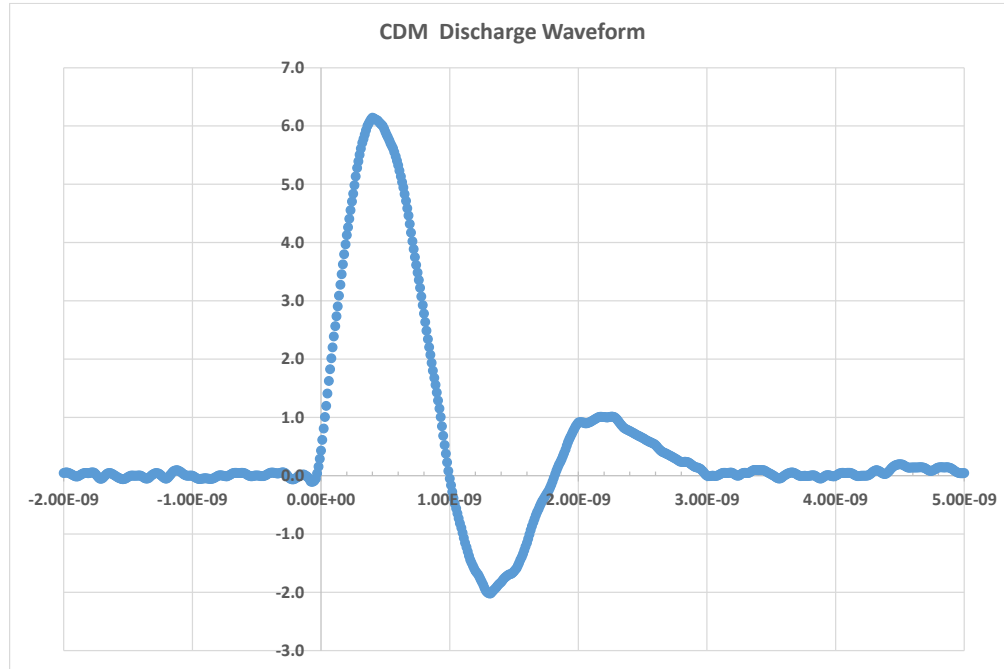


Figure 57: Typical CDM Waveform as Measured on an Oscilloscope

Since the current is a measure of the change of charge with time, it is possible to calculate the total charge, and therefore the effective capacitance (C_{eff}) of a pin under test with the captured current waveform by first extracting the charge (Q) using the equations:

$$I = \frac{dQ}{dt} \quad (3)$$

and

$$Q = \int_0^t I(t)dt \quad (4)$$

Numerical analysis can be completed using the trapezoid rule for approximating the definite integral shown in (4) and works by approximating the region under the graph of the function $I(t)$ as a trapezoid and calculating its area. The integral can be better approximated by partitioning the integration interval into smaller time segments and then applying the trapezoidal rule to each subinterval of time and summing the results. The approximation becomes more accurate as the resolution of the partition increases. Using the typical time steps captured on a high bandwidth oscilloscope can accurately measure the total charge (Q).

Once Q has been calculated, C_{eff} can be calculated directly using equation (2) knowing the plate voltage. Note, if using the factor/offset approach for the CDM system, the voltage is not the software voltage but the actual voltage on the field plate, taking into account factor/offset.

Why is this information useful? How can it be used? In some cases, the failure seen in CDM testing may not be a function of the I_p . It may be a function of the total charge Q delivered at the charging voltage. Knowing how to calculate the charge Q allows direct quantification of failure risk as a function of Q. Additionally, understanding I_p as a function of package size can be useful when

discussing data sharing opportunities and risks when a die goes from one package size to another. While peak current as a function of package size (using X/Y dimensions) is a good first-order evaluation, peak current versus C_{eff} is a much better way to understand the risks when considering data sharing for CDM.

11.0 SINGLE DISCHARGE VERSUS DUAL DISCHARGE METHOD SELECTION

See ANSI/ESDA/JEDEC JS-002 Annex H for detailed descriptions and graphics of both FICDM tester operation methods, which most testers are equipped to perform. There are some practical advantages unique to each method, but both are valid, and if the tester is calibrated correctly, the resultant stress is equivalent.

Single Discharge:

1. It allows for single polarity stressing, which is necessary if partitioning samples by polarity and debugging polarity failure sensitivity.
2. Has risk for generating either under-stress or over-stress waveforms due to no-connect pin residual charge effects. See Section 12.2 for explanation and mitigation suggestions.

Dual Discharge:

1. Results in both polarity stresses for connected pins.
2. Results in single polarity stress for no-connected pins (see Section 12.3).
3. Up to 20% faster for 1x pulse/pin (ANSI/ESDA/JEDEC JS-002) and up to 40% faster for 3x pulses/pin (AEC Q100-011).

12.0 NO-CONNECT PIN TESTING CONSIDERATIONS

When planning and performing CDM testing on device packages that include no-connect pins (NC), there are several items to consider, such as:

- successful pulse detection, I_p logging, and event detectors
- over-stress and under-stress risks on adjacent connected pins, and possible incorrect qualification
- choosing the correct discharge method for no-connect pins

No-connects are required to be tested in ANSI/ESDA/JEDEC JS-002. There is no exemption for no-connect pins, as there is for HBM (ANSI/ESDA/JEDEC JS-001) testing. However, a recent case study has shown that CDM stress applied to a no-connect pin can sometimes result in damage to a physically adjacent circuit. [9]

12.1 Pulse Detection, I_p Logging, and Event Detectors

Many CDM testers contain an event detector designed to help identify when a failure to discharge occurs and may require a pin retest. Sometimes this can occur if a pogo pin does not extend far enough to contact a ball, pin, or test pad. It can also happen on no-connects and also on connected pins of very small package devices.

It is known from CDM peak current (I_p) logging that no-connect pins generate a very small discharge event. The size of this runt pulse varies based on package size, as shown below in Figures 58 and 59, smaller packages have a higher chance of triggering false event detections. The runt pulse size also varies as a function of the magnitude of the charging voltage. Consequently, the number of potential false event detections increases at lower test voltages.

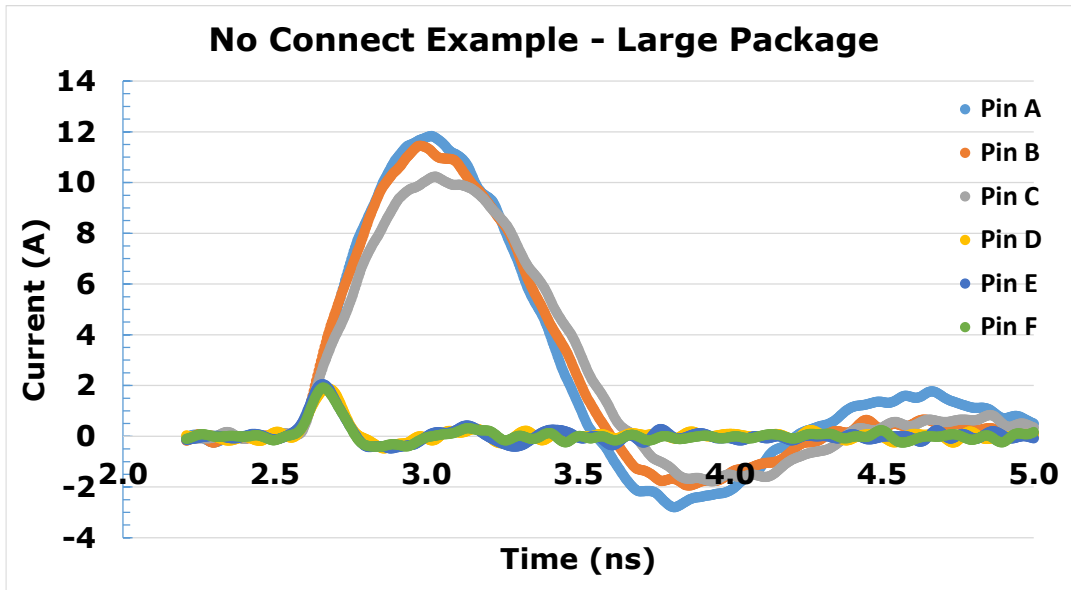


Figure 58: *Ip* Logging on a Larger (52.5 mm x 51 mm) Package Looking at Three Valid IO Pins (A, B, C) and Three No-Connect Pins (D, E, F) at 500 Volts

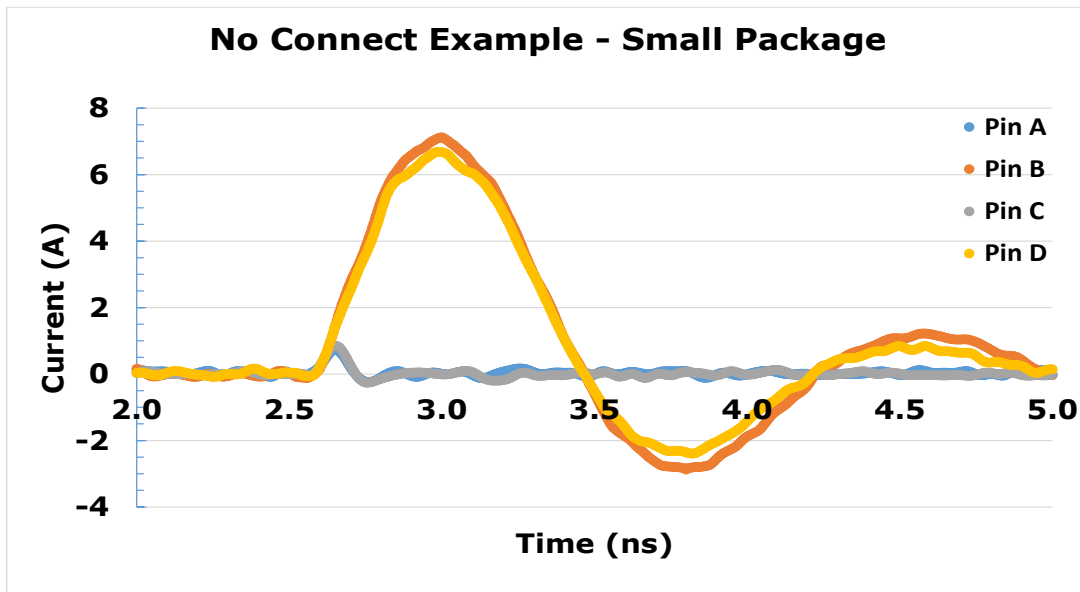


Figure 59: *Ip* Logging on a Smaller (15 mm x 15 mm) Package Looking at Two Valid IO Pins (B, D) and Two No-Connect Pins (A, C) at 500 Volts

NOTE: The CDM tester event detector should not be used as a sole means of ensuring a valid *Ip* pulse on each pin. A valid *Ip* should be captured by oscilloscope from the discharge waveform during testing and logged for later review.

Suggested methods for addressing false event detector trigger fails:

1. If connected pins and no-connects are tested simultaneously, review the number of failures identified by the CDM tester. If the number of failing pins corresponds to the number of no-connects (or less), then re-testing is likely not required. However, this approach does not

- guarantee that all the “connected” pins got discharged properly and can lead to the potential risk that the test was not run correctly and should be used cautiously.
- During the CDM test, log the I_p discharge and analyze the results afterward to determine if any “connected” pins received a poor discharge and verify that only the no-connects saw the runt pulse. This method, though, is time consuming and does require that I_p logging is available and enabled.
 - Test the connected pins in a separate run from the no-connects. Any event detector trigger failures during the connected pin test should result in a retest of the failing pins. Any event detector triggers during the no-connect group testing would not require a re-test. This last approach is typically the cleanest and easiest way to address the issue.

12.2 Over-Stress/Under-Stress Risk When Zapping No-Connects

When testing no-connect pins, it has been observed at higher charging voltage levels that a residual charge can remain on the device and result in either an under-stress or over-stress waveform on the connected pin immediately following the no-connect. Figure 60 demonstrates how residual charge can cause increased total charge stress and higher I_p on the subsequent connected pin, potentially causing it to fail at a lower TC level than a similar pin not adjacent to a no-connect pin.

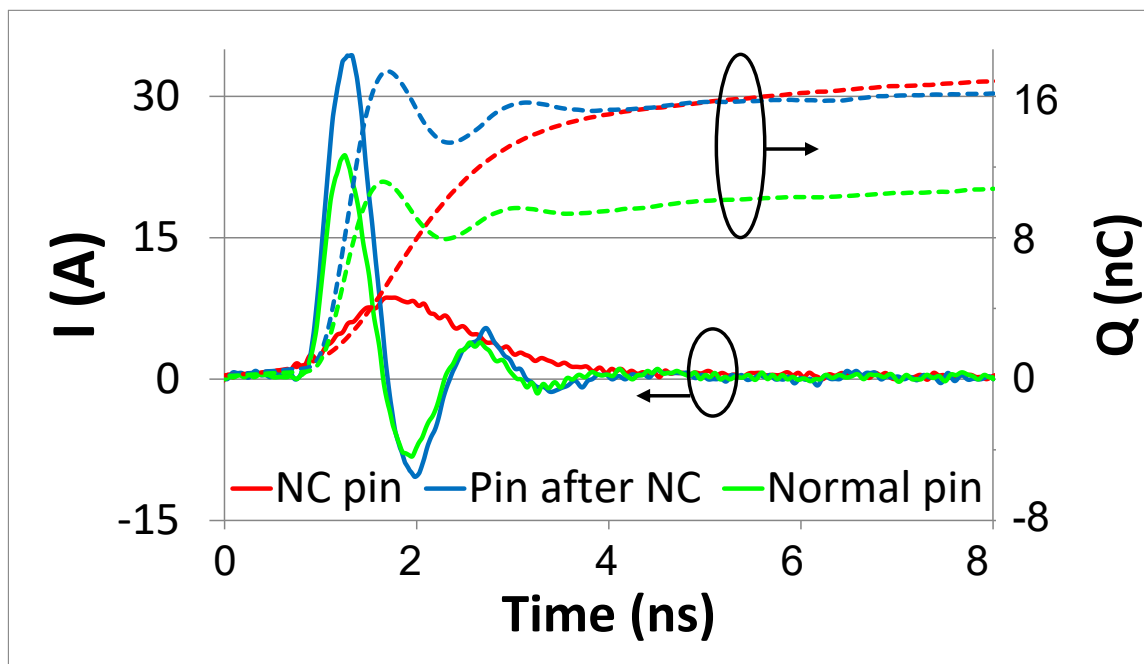


Figure 60: Comparison of Current (Solid) and Charge of NC Pin and Two Subsequent Pins

The route of charge transfer during stress on a no-connect pin can be external to an adjacent ball or pin, or it can be internal to the package through a dielectric breakdown to an adjacent conductor or circuit.

The polarity and CDM tester operational mode affects the next connected pin, as shown in Table 7. For example, if the CDM tester is running in single discharge mode and a no-connect pin is zapped negative (-), the effect on the following connected pin can create an under-stress condition when that next pin is zapped negative (-). Or if the CDM tester is running in single discharge mode, and a no-connect pin is zapped positive (+), then negative (-), the effect on the following connected pin can create an over-stress condition when that connected pin is zapped positive as part of the positive then negative (+-) sequence.

Table 7. Effect on the Connected Pin Immediately Following a No-Connect Pin at High Charge Level [9]

CDM Discharge Mode	Polarity	Effect on Pin following NC
Single	+	Under-Stress +
	-	Under-Stress -
	+-	Over-Stress +
	-+	Over-Stress -
Dual	+-	Under-Stress +
	-+	Under-Stress -

To avoid or minimize this undesired effect while still meeting the requirement to test all no-connects, utilizing one or more of the following mitigation methods is suggested:

1. Perform a 0-volt discharge for every connected pin after stressing a no-connect pin
2. Stress no-connect pins at the end of the test sequence
3. Stress no-connect pins on separate samples from connected pins

12.3 Choosing the Correct Discharge Method for No-Connect Pins

Figure 61(a-c) below compares the voltage stress and discharge events for a connected pin and a no-connect pin during a single dual discharge method (DDM) test cycle.

For a connected pin (Figure 61b), the discharge event (3) when the pogo first touches down and the field plate is positive results in a flow of charge to the device (3-4). When the pogo is lifted (4), the charge is trapped on the part (5-6), and when the field plate voltage returns to 0 volts, inverse stress across the part is achieved, allowing for an opposite polarity event when the pogo pin touches down for the second time (6). When stressing a no-connect pin (Figure 61c) with DDM, there is no path for discharge current to flow at lower TC levels (3), and consequently, there is no polarity stress reversal (5-6). This results in single polarity stress only. For a no-connect pin to receive both required polarity stresses, either run a separate DDM for each polarity (+/- and -/+) or run two single discharge method (SDM) cycles (+ and -).

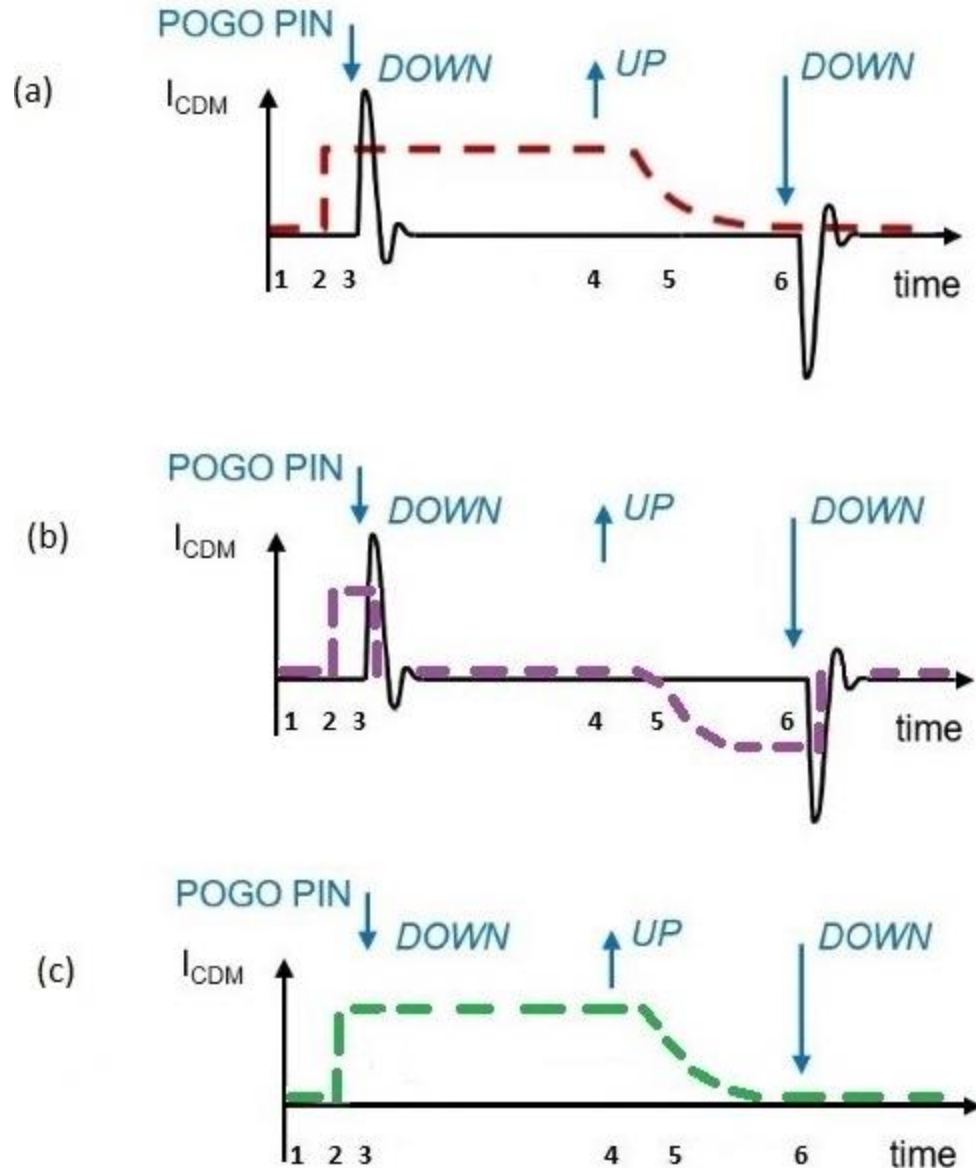


Figure 61: Dual Discharge Event for Connected and No-Connect Pins

- a) --- Field charge plate voltage when stressing a connected pin
- b) --- DUT voltage when stressing a connected pin
- c) --- DUT voltage when stressing a no-connect pin (note: no I_{CDM} event)

13.0 FIRST PIN TESTED WAVEFORM

It has been observed that the first contacted pin on a part may receive either a higher or lower than expected I_p waveform [10]. After this first contacted pin has been pulsed one time, any remaining pulses on that pin have I_p waveforms of expected magnitude. One reason for this phenomenon is tribo-charging of the DUT and/or tester insulator (FR4 material is highly charging). When the first contacted pin received its first pulse, the combined effect of the field plate E-field and the trapped charge on the insulator/part can add or subtract and result in an under-stress or over-stress waveform. After this first discharge, any E-field due to charge on the insulator/package surface is neutralized by an opposite charge on the device conducting surfaces. If calibration coins are

handled using insulative tweezers, the same phenomena can present during calibration on the first pulse and distort the average I_p .

To avoid or minimize this undesired effect, consider one or more of the following mitigation methods:

1. Contact a pin with robust ESD protection before starting the test sequence as part of the DUT alignment process.
2. If the tester allows, perform a 0-volt discharge on 1st connected pin in the test sequence before stressing that pin with a test voltage.
3. Use dissipative tweezers and touch pins of the DUT after sliding into position to neutralize tribo-charge via a grounded operator.
4. Staticide on top of FR4 reduces the tribo-charging effect but can be short lasting as any cleaning with isopropanol removes the residual staticide.
5. Avoid using insulative tweezers, especially with calibration coins.

14.0 SMALL PACKAGE PARTS AND CDM

ANSI/ESDA/JEDEC JS-002 has two sections, Section 7.5 and Annex C, addressing small package products and limitations they bring to CDM testing. Annex C defines an optional procedure for establishing an integrated circuit capacitance C_{Small} for specific technology and design flow. For devices with capacitance below C_{Small} , CDM testing is no longer required if several design and testing requirements are met. Integrated circuits and discrete semiconductors (ICDS) with capacitance below C_{Small} and which satisfy the requirements of Annex C shall be considered to have a CDM passing level of TC 750 (Classification Level C2b in Table 2 of ANSI/ESDA/JEDEC JS-002). These can be exempt from CDM testing.

For CDM purposes, small packages are generally defined as products having a package size of 16 mm² or less. These can be difficult to align in field-induced testers, particularly if they are chip-scale packages. Alignment difficulties can result from being unable to image the product for pogo/IC pin alignment and the use of some “holding” material to keep it from moving, ensuring the DUT is lying flat atop the field plate dielectric.

One possible method is to use FR4-based “holders” cut out to the package's size to allow the DUT to be held within the opening or align on edges with the tester DUT alignment bracket shown in Figure 62. These holders can be difficult to mill the shape, and care must be taken. If a hole or cutout is used, one must also be aware of the FR4 thickness. If the FR4 is too thick, the alignment along the edges of the package (particularly WCSP) can physically hinder the pogo from an appropriate landing on the pin. The X-Y dimensions should also be slightly larger, at least 10%, in both the X and Y dimensions. Most CDM test equipment available on the market also have alignment brackets or full frames. To avoid the pogo pin touching the edges of the FR4 support template and the FR4 “L” bracket or FR4 frame (depending on the tool being used), thinning of these structures is needed. The FR4 pieces can be reduced on the edges or throughout the pieces.

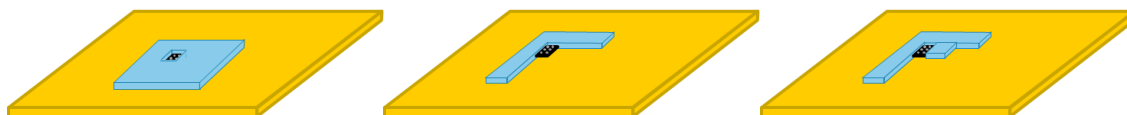


Figure 62: Examples of Securing a Package Using FR4-Based “Holders”

When the vacuum hole is $\geq 20\%$ of the package area [11], the package should be moved from the vacuum hole to another location on the field plate. This generally means that packages 4 mm² and less should be moved off the vacuum hole. Another consideration for mechanical stability (tilting or X-Y movement) is that if the vacuum hole's width is 70% or more of either the X or Y dimension, moving the part off the vacuum hole is recommended. An FR4 holder, sometimes with a notch in the corner with the holder over the vacuum hole, can be used to keep the part in its new position anchored against another piece of FR4 during the test. Since the vacuum does not hold the

package, care must be taken to minimize the pogo pin's downward force to not cause a change in position, which may nullify the stress test. Since the CDM test equipment available has alignment brackets or full frames that, along with the holders mentioned above, work as a system to keep different types of small packages in position. The FR4 holder's effect on the I_p is, as described in [11], approximately a 10% increase (template/no template = 1.095). This range is within the margin of error of FICDM peak current, as shown in Figure 63.

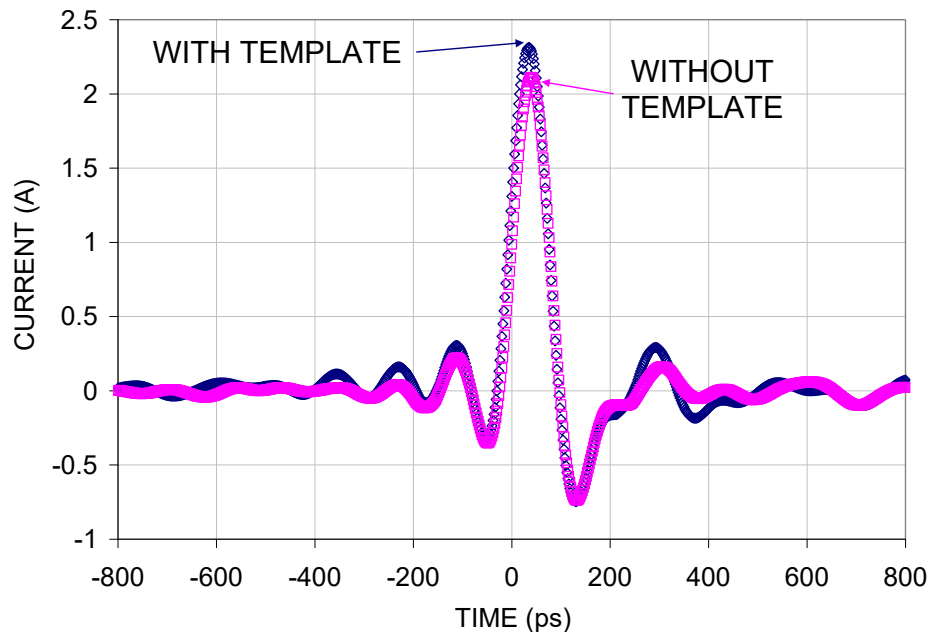


Figure 63: Impact of Template Holders on CDM I_p [10]

There are situations where it is more convenient for reliability testing to put small packaged products on carrier boards to simplify handling. Care must also be taken to verify that the part remains in contact with the field plate (see Figure 64(a) and 64(b)). CDM stress on products mounted on carrier boards can also create an additional charge and generally higher stress than possible without the carrier boards [11]. The peak current increase may be 20x or higher. Depending on the mounted device area, one should move the setup off the vacuum hole. See below for more details.

14.1 Small Packages with Gull-Wing Leads

Small packages with gull-wing leads can be very difficult to stress. These packages may be more difficult to stress than most WCSP devices. The package mass is small, along with the package surface area. The most common small leaded packages are SOT23 (all incarnations) and SC70. Figures 64 & 65 below show the four options available to stress devices in these packages.

A SOT23 example is shown in Figure 64. Figure 64(a) shows the package sitting on the vacuum hole. The vacuum hole area (0.785 mm^2) compared to the area of the SOT23's is about 20%. The SOT23 dimensions are $W = 1.6 \text{ mm}$ and $L = 2.9 \text{ mm}$. Also, the vacuum hole diameter is a significant portion of the width (1.6 mm). Moving it off the vacuum hole may be a good idea; Figure 64(b). Using an FR4 support template gives more stability during stressing. If one would choose not to use an FR4 support template, care must be taken to have as light a pogo pin touch as is possible. However, the possibility of the part tilting is high. If the part tilts, the primary risk is the ESD tester losing alignment with the package, increasing the likelihood of runt pulses or no pulse for all pins tested after the tilt. Using a support template gives the user additional control of the package. Even using the support template still does not change the concept of vacuum hole influence. Even with

a support template, the small package width offers little support over the vacuum hole and can result in a slight tilting of the package (even in the support template), causing potential runt pulses or no stress at all.

The SC70 (Figure 65) is a smaller version of the SOT23. Its package dimensions are $W = 1.25$ mm and $L = 2.0$ mm. The area in comparison to a vacuum hole area is 31%. This value is above the 20% limit and should be stressed away from the vacuum hole. Also, this package does not have enough mass to realistically maintain its position with a pogo pin touch. A support template is highly recommended and the best way to get reliable stress.

Any time support templates are used, care must be taken to evaluate the support template's thickness to ensure the package surface is in contact with the field plate dielectric. Any air gap lessens the stress. For these package types, use Figure 64(d) for SOT 23 and Figure 65(d) for SC70 for the best results relative to stability and consistent CDM stress.



Figure 64: Examples of SOT23 With and Without Placement on Vacuum Hole

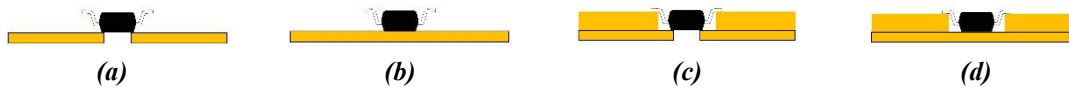


Figure 65: Examples of SC70 With and Without Placement on Vacuum Hole

15.0 DIFFICULT TO TEST PACKAGES - TIP OVER POTENTIAL

Long lead packages, packages with a surface that is not regular (for example, unmolded), or BGA with a small IC can be misaligned by the pogo pin touching the balls away from the center or the end of the lead.

Also, in this case, a cut-out to size holder can be a possible solution, but it is preferable to use FR4 shims. The shims should cover as little surface or lead as possible (see Figure 66). Peak current evaluations with and without the shims are suggested to ensure the package is making solid contact with the field plate's surface.

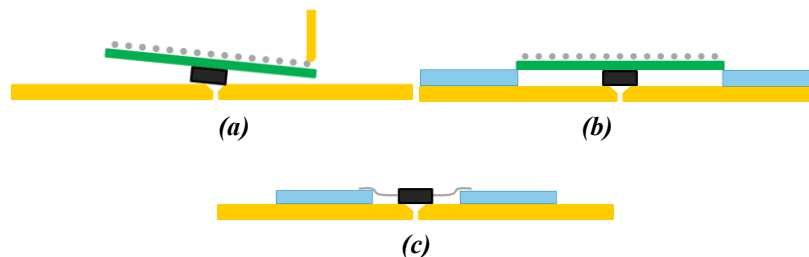


Figure 66: Examples of Holding a Package in Place With Risk of Tipping

15.1 TOxxx Packages

TOxxx packages have a big tab for power dissipation and straight leads; thus, it is possible to place these with tab up or down on the field plate, as shown in Figure 67. This simple difference can lead to a completely different qualification level because the total capacitance is bigger when the device is seated tab down, as shown in the I_p versus charging voltage graph in Figure 68.

It is suggested to test such parts tab up for testing conformity with quad packages that generally have the slug on the bottom of the package with other leads and are therefore CDM tested in the slug up position. The tab is generally connected to one of the pins (the central one is the most common), so the tab test can be avoided (evidence of connection should be included in the report).

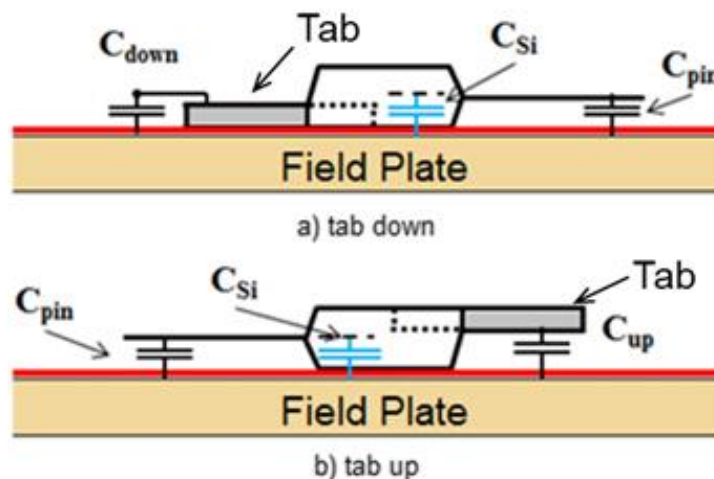


Figure 67: TOxxx Package

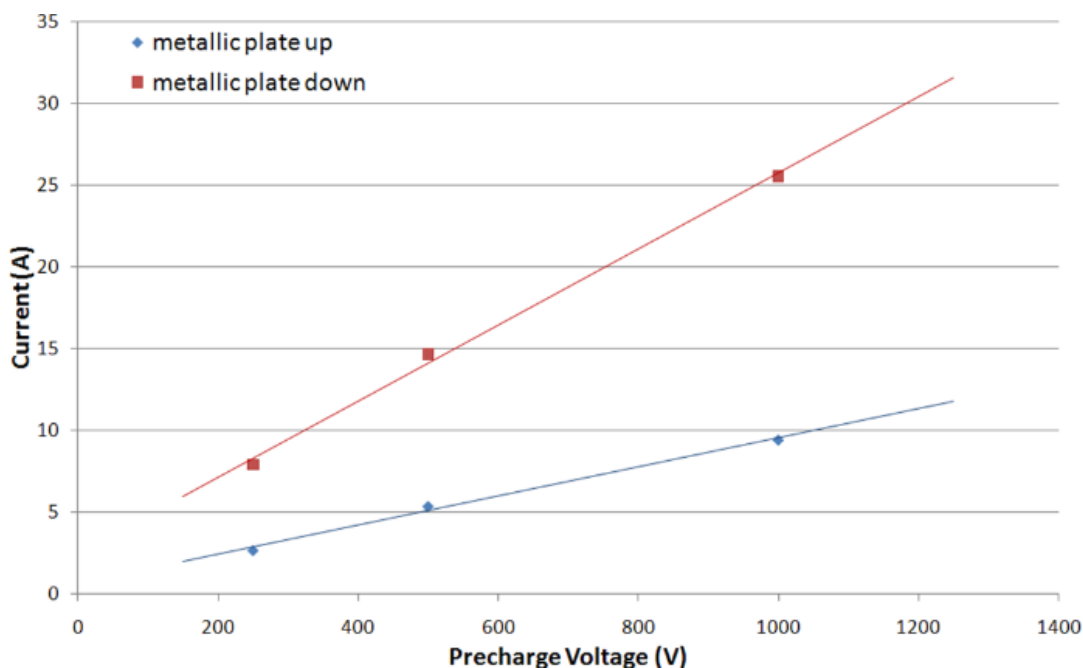


Figure 68: I_p Versus Charging Voltage of TOxxx Package – Tab Up Versus Down

15.2 Multi-Watt Packages

Multi-watt packages have long leads bent at different heights, as shown in Figure 69. If the pogo is long enough to avoid the ground plate touching the leads, it is possible to test them, paying attention that the CDM tester is capable of recognizing the different pin heights and raising the pogo pin to a level higher than the highest pin before moving horizontally.

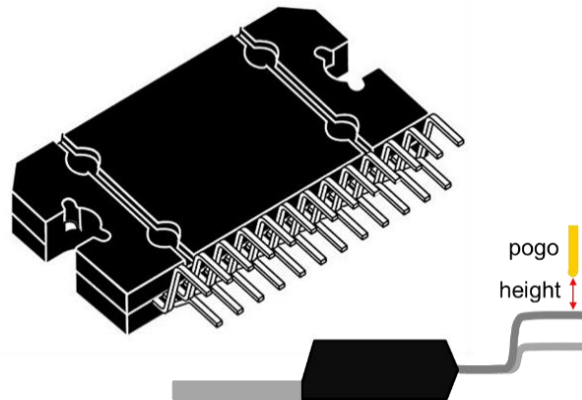


Figure 69: Multi-Watt Package

If the pogo pin is not long enough, one way is to bend the leads pressing them on an ESD surface, as shown in Figure 70.

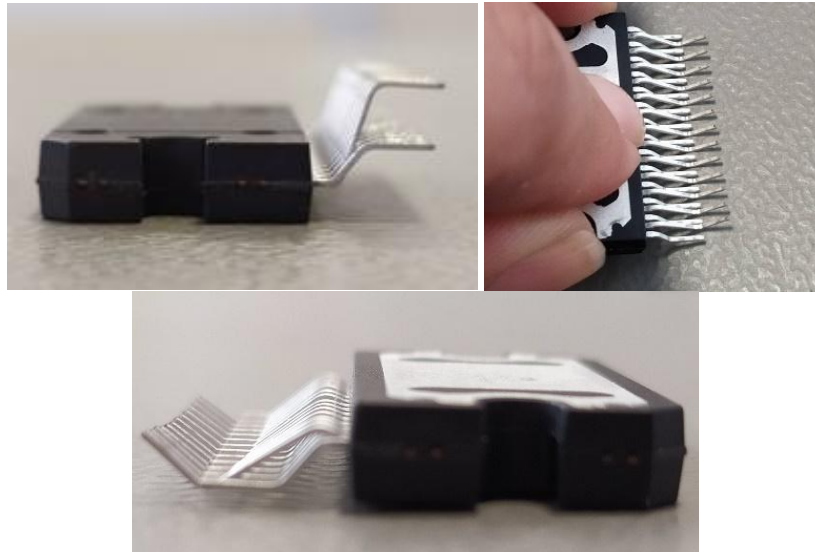


Figure 70: Bending Package Leads to Alter the Pin Height

NOTE: The operator should be grounded before touching the unit.

Parts should be loaded “tab up” to be able to touch the leads near the package, as shown in Figure 71.



Figure 71: Pogo Pin Landing on Adjusted Lead

To restore the leads at the end of the CDM testing, gently push on the ESD mat rotating the part to adjust leads back to the original height, as shown in Figure 72. A socket can be used to further restore the leads to the original position.

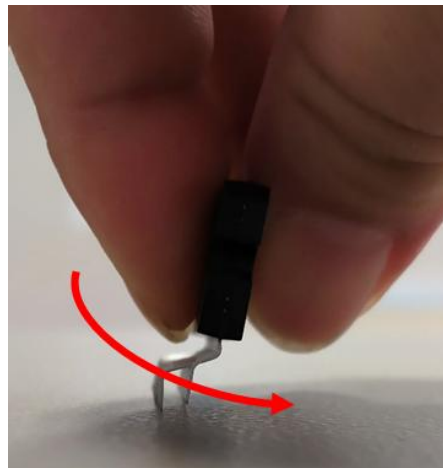


Figure 72: Adjusting Leads Back to Original Height on ESD Mat

NOTE: The operator should be grounded before touching the unit.

In this case, the tab is generally connected to one of the pins, so the tab test can be avoided (evidence of connection should be included in the report).

15.3 Thick Packages

Packages can sometimes be so thick that the pogo pin cannot touch the leads without touching the package or other leads, as shown in Figure 73.

In this case, it is suggested to use a pogo pin with a different length or slightly bend the leads to allow the pogo pin to contact.

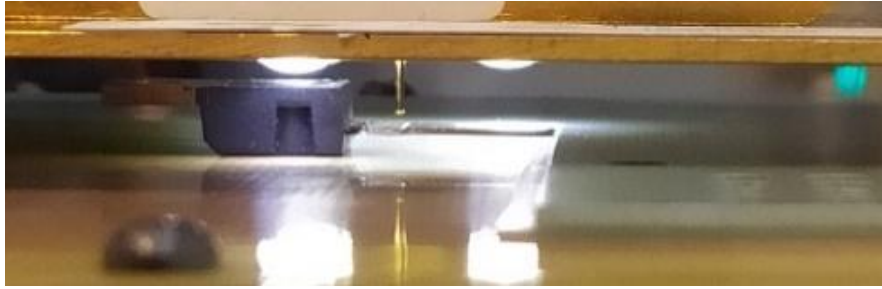


Figure 73: Thick Package Limiting Pogo Pin from Landing on Lead

15.4 Long Lead Packages

Packages with long leads (for example, flat pack) can have different peak current and rise times depending on pogo pin landing location because of lead inductance. Figure 74 depicts two landing positions on a TO220 package, and Table 8 shows data at 500 volts for the pogo pin at the lead end and the package with the tab up or down.

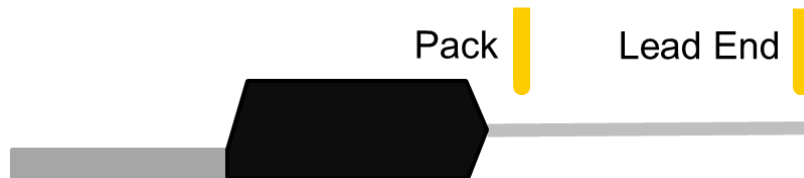


Figure 74: TO220 Package Depicting Pogo Landing Locations

Table 8. I_p Data for Various Landing Positions of the Pogo

Tab	Position	I_p [amperes]	T_r [ps]	FWHM [ps]	Q [nC]
DOWN	Lead End	5.30	337.7	676.1	3.57
DOWN	Pack	6.07	271.5	577.2	3.47
UP	Lead End	3.46	208.8	368.7	1.27
UP	Pack	3.65	227.7	361.8	1.31

For CDM testing, such as FICDM, where the charge is removed from the device by grounding the leads, this long lead issue is not a concern because internal rise time is driven by package geometry. In contrast, for any stress externally forcing rise time (such as CC-TLP or a contact CDM), the lead inductance can play a significant role [12].

15.5 Exposed Metal Plates and Heat Sinks

Some packages, including many power devices, have one or more metallic plates connected to the silicon (see Figure 75). Sometimes these are thermally connected but electrically floating.

Often connected to the silicon substrate, these exposed metal plates act either as a heat sink or facilitate current recirculation. In some cases, they are connected to power supplies or high current connections.

These exposed metal areas should be CDM tested if physically possible, orienting the package as appropriate. In some cases, the terminal is on the device's top surface to allow a fan to be mounted

on top of the heat sink. Therefore, the only way to perform the CDM is to place the parts live bug on the field plate and test only the terminal in this configuration, while all other pins or balls should be tested in dead bug mode as usual.

Non-standard part orientation for products with these special case terminals should be documented in the final report.

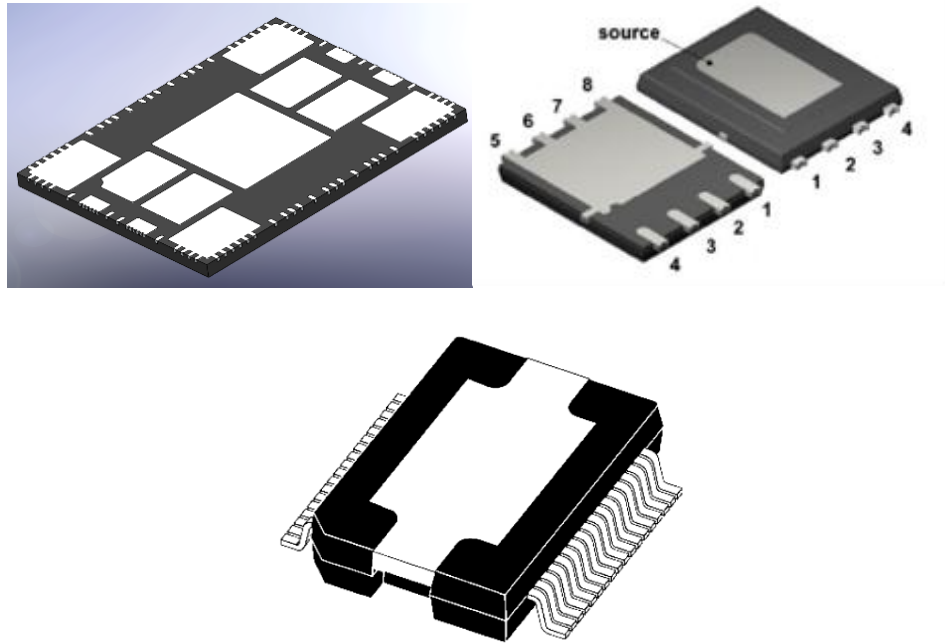


Figure 75: Examples of Product with an Exposed Metal Plate/Heat Sink

15.6 Test Pads and Pins Designated as No-Connect (NC) or Do-Not-Use (DNU)

In some packages, there are terminals intended for debugging or testing purposes by the IC vendor only. These may be designated DNU, or NC, with instructions to 'connect to VSS' or 'leave floating'. In some cases, pins are also cut or solder balls not placed on pads to ensure the customer cannot electrically connect them (see Figure 76).

Examples are sensing connections for internal voltage, programming connections, internal daisy chain signals, test mode signals, etc.

If possible, such terminals should be CDM tested, paying attention that height or position can differ from regular terminals.

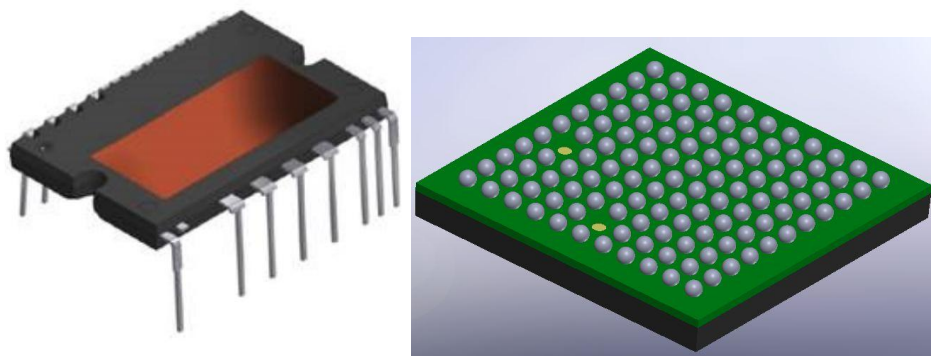


Figure 76: Examples of Product with Pin/Balls Removed to Avoid Customer Use

16.0 CDM DATA REPORTING

EOS/ESD Association, Inc. published a standard practice (industry recommendation best practice) document, ANSI/ESD SP5.0 (Reporting ESD Withstand Voltages on Datasheets) [13]. This document provides a standardized approach and template to include device-level ESD withstand levels in datasheets or other similar product information documentation.

The approach and template in ANSI/ESD SP5.0 also provide information for elaborating on the device's ESD performance. This can be useful when a supplier wants to convey information that gives additional information about relative ESD risk, identification of the most sensitive device pins, or discussion of performance relative to ESD targets of a given device family or technology. Finally, the template includes language that clarifies CDM withstand thresholds are relevant only to handling in an ESD protective area (EPA). These ratings do not predict and are not relevant to performance at the system level.

An example of CDM reporting using the template is as follows (with the referenced standard).

ESD Information for Handling of ESDS Devices in an ESD-Protected Area

CDM (ANSI/ESDA/JEDEC JS-002-2022): 250 V; Class C1

NOTE: All pins pass 500 volts CDM except high-speed pins 3-4, which pass 250 volts CDM

The reporting of “exception pins” such as pins 3-4 in the example above is critical for a manufacturing facility to know about the need for particular manufacturing ESD control procedures, such as those outlined in ANSI/ESD S20.20.

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